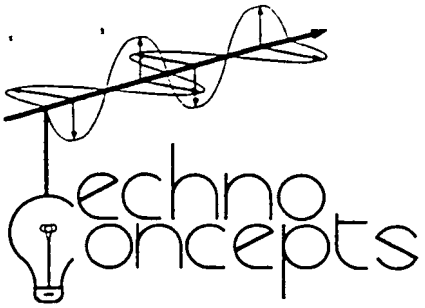
Exhibit 1



A Digital I-Q Demodulator for PCS

Final Report of the Study Covering the Period
April through July, 1995

Presented to Omnipoint Corporation

July 20, 1995

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1. Abstract

In this study, the design for a completely digital I-Q demodulator was developed. Based upon sigma-delta A/D converter technology developed by TechnoConcepts, Inc., the proposed design utilizes a double-sampled GaAs 1-bit sigma-delta modulator operating at an effective sample rate of approximately 4 Gigasamples per second. The output of this GaAs modulator is processed using a silicon CMOS IC that smoothes the output of the modulator and performs coherent I-Q demodulation. The combined power dissipation for the two ICs is estimated to be less than 700 mW.

2. Background

2.1. Objective of the Effort

The objective of this effort is to develop a low power (approximately 300 mW) digital receiver front end to demodulate a signal with the following characteristics:

Signal input frequency	1890 - 1990 MHz
Modulation bandwidth	2.5 MHz
Receiver input dynamic range	84.3 dB (14 bits)
Maximum input signal amplitude	+ 10 dBm

The proposed design utilizes two integrated circuits: one GaAs and one silicon. The following are preliminary specifications for the two components:

Supply voltages	5 (5.2?)V GaAs; 3.3V silicon
Power Dissipation	≈ 500 mW (total)
Output sample rate	≈ 10 Mb/s
Data interface rate between GaAs and silicon ICs	≈ 125 Mb/s (× 32 bits)

2.2. Sigma-Delta A/D Conversion

Sigma-delta (or more properly delta-sigma) converters are based upon the principle of making multiple coarse estimates to an input voltage through a feedback loop and making corrections to these estimates based upon the cumulative error of these estimates. In this sense, the sigma-delta converter is analogous to a Type II phaselocked loop. A sigma-delta converter actually consists of two parts: a modulator, or the feedback loop that makes the coarse estimates, and a filter/decimator which smoothes the output of the modulator through a weighted averaging operation. The block diagram of a simple sigma-delta converter appears in Fig. 2.2.1. The transfer function of this block diagram is easily recognized as:

$$H(s) \equiv \frac{Y(s)}{X(s)} = \frac{A \cdot F(s)}{1 + A \cdot F(s)}$$

In the limit as the input frequency tends to "DC" (which is equivalent to the case where the sample frequency, fs, tends to infinity), the output (Y) of the converter (after suitably

averaging a sufficient number of samples) will tend toward becoming an arbitrarily close estimate of X. The ultimate resolution of such converters is thus not limited by the resolution of the ADC within the loop; rather it is limited by the following:

- The precision of the DAC (and not the resolution)
- The loop filter function F(s) and the loop gain A
- The ratio between the sample rate of the ADC (fs) and the input bandwidth of X.
- The frequency response of the filter following the modulator.

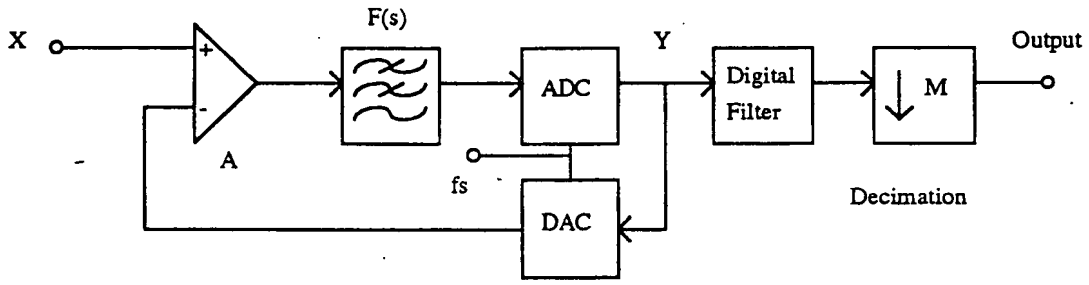


Fig. 2.2.1. Block diagram of a simple sigma-delta converter.

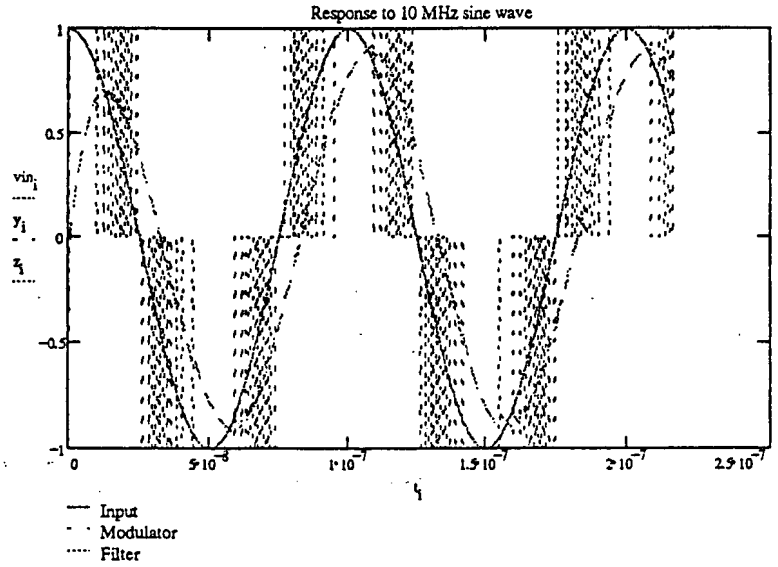


Fig. 2.2.2. Response of a sigma-delta modulator to a 10 MHz sine wave. Sampling frequency is 4 Gs/s. The solid trace is the input signal. The dotted trace is the modulator response. The dashed trace is the result of passing the modulator response through a single pole filter.

A representative simulation of a simple sigma-delta converter is shown in Fig. 2.2.2. In the simulation, a one volt amplitude sine wave serves as the input; the sampling frequency is approximately 4 Gs/s (2 Gs/s operating on two phases). During each of the two phases, a one bit estimate of the loop error is generated. Thus the output code word has three states (both low, one output high, and both high). The solid trace shows the input signal. The three valued output of the modulator appears as a dotted trace. Finally, the dashed

line represents this coarse output after having been fed through a lowpass filter (in this case, a single pole with a 3 dB point at 20 MHz). Note the smoothness of the sine wave.

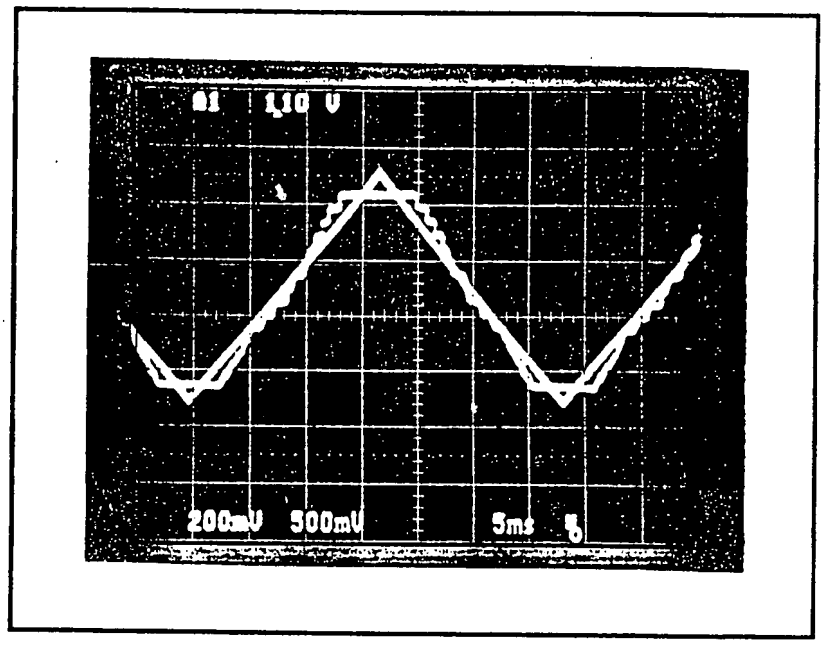
GaAs sigma-delta converters are the optimum solution for demodulating the 2.5 Mb/s baseband data. Sigma-delta converters, because of their inherent precision are capable of achieving higher resolutions than flash converters; GaAs technology because of it inherent bandwidth is capable of implementing high clock rate modulators that generate more than one thousand samples per bit period. In the following section, we will discuss TechnoConcepts' previous experience in developing GaAs sigma-delta A/D converters.

2.3. Previous Work

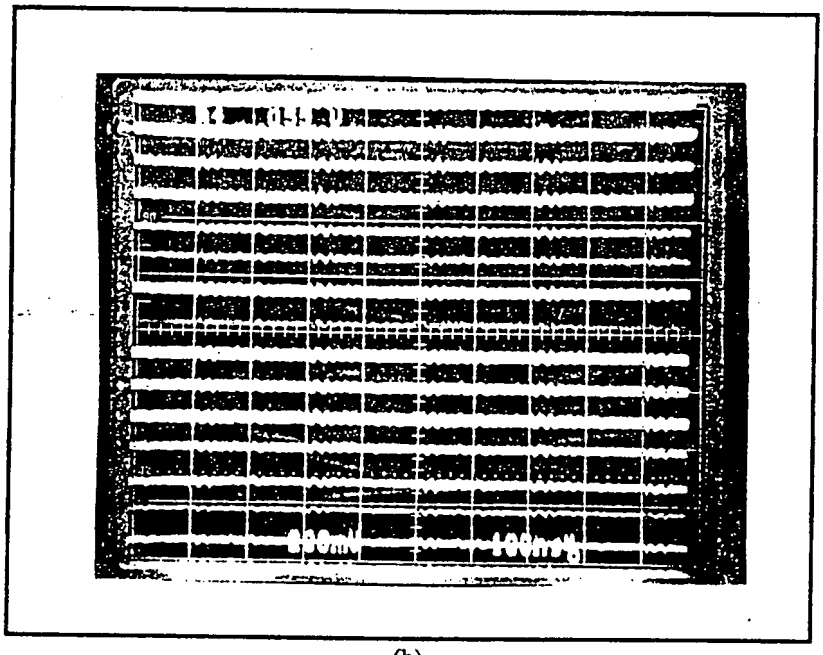
TechnoConcepts, Inc. has been involved with the development of GaAs and silicon integrated circuits since its inception in 1991. The sigma-delta converter effort has been ongoing since 1992. Funded by contracts from the U.S. Department of Energy and other customers, TechnoConcepts has successfully demonstrated a 1.6 GHz clock rate four-bit modulator (wherein each coarse estimate has four-bit resolution instead of one) and has developed many proprietary designs including those for which patents are pending.

A plot of the four-bit sigma-delta modulator response is shown in Fig. 2.3.1. In the test circuit, the digital output has been fed into a four-bit DAC for ease of measurement. In Fig. 2.3.1(a), the modulator output is superimposed upon the input signal (a 30 Hz sawtooth wave used for ease of visual comparison). In Fig. 2.3.1(b), the individual values of the internal DAC are shown in order to demonstrate its linearity and precision. Additional results have been demonstrated using input signals in excess of 10 MHz at the full clock rate of 1.6 GHz captured with a 20 GHz bandwidth sampling oscilloscope.

Additional characterization work is in progress on a monolithic 16-bit A/D converter utilizing three stages, each with four-bit resolution. Work is also in progress on a single-stage modulator using four-phase sampling for defense applications. The proposed converter for this effort comprises a scaling back in both complexity and size compared to our previous endeavors in order to minimize the finished cost of the final product.



(a)



(b)

Fig. 2.3.1. Response of a four-bit sigma-delta modulator to a low speed sawtooth waveform. (a) The input signal to the modulator superimposed upon the output signal from the modulator. (b) The same response expanded in time to show the sixteen evenly spaced output levels of the internal DAC.

3. Results of the Study

3.1. Summary of the Findings

In this study, several options for implementing a digital I-Q demodulator were explored. Among the alternative implementations considered were:

- A downconverting sigma-delta modulator in which the input signal is first converted to an intermediate frequency (IF) then digitized and demodulated.
- A direct conversion A/D converter in which the modulated carrier is directly digitized then demodulated.
- A demodulator/digitizer in which the I/Q demodulation is performed then each of the output channels (I and Q) are individually digitized and processed.

The third alternative was considered and rejected because we felt that the analog I-Q demodulation would be unacceptable in light of the required resolution. We also viewed the second alternative as unacceptable since the combination of the required modulator resolution and sample rate necessary to achieve the desired overall resolution was impractical for implementation using less expensive GaAs MESFET (versus HBT) technology. Thus we concluded that the most practical alternative is the first one. We expect this to be the least expensive one as well since the critical high speed portion of the converter would be implemented using a medium scale integration (MSI) GaAs chip while the complex digital filtering and demodulating functions would be relegated to an inexpensive silicon CMOS chip.

3.2. Overall Block Diagram

A block diagram of the proposed digital I-Q demodulator appears in Fig. 3.2.1. In this design, the clock frequency (approximately 2 GHz) is offset from the incoming carrier frequency by approximately 10 MHz. As a result, the signal is translated down to an intermediate frequency (IF) of approximately 10 MHz at the input stage. This translated signal is double-sampled (at each half clock period) resulting in an effective sample rate of about 4 Gs/s. In order to avoid having to implement a large FIR within the GaAs chip, the high speed data is immediately time-division demultiplexed to create 32-bit wide words updating at a rate of approximately 125 MHz.

The silicon signal processing chip performs three functions. First it implements a steep anti-aliasing filter (320 taps) which ensures that all signals in excess of approximately 62.5 MHz bandwidth are attenuated. Second, it performs a non-integer sample rate change intended to adjust the sample rate to be exactly four times the effective IF frequency. Finally, it extracts the I and Q data from the IF signal and presents them to the I and Q output ports with 14 bit resolution.

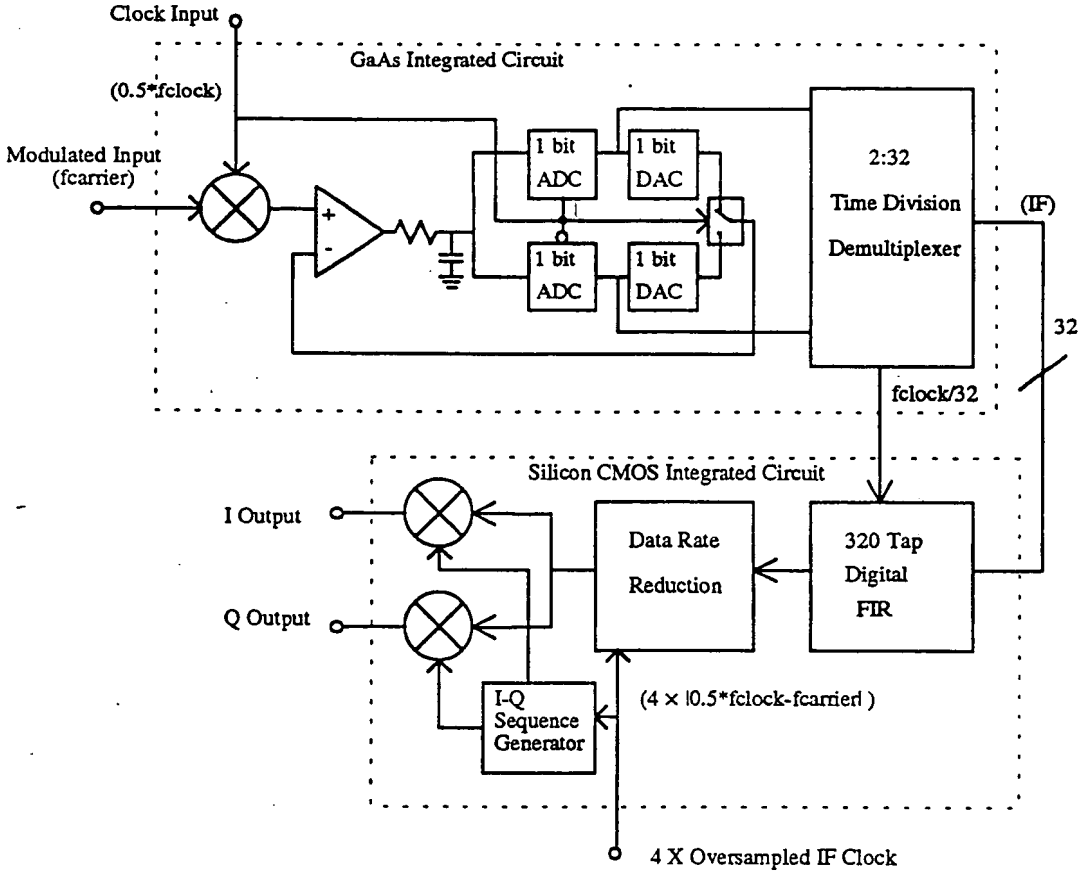


Fig. 2.3.1. Block diagram of the proposed digital I-Q demodulator. The demodulator consists of two components: a GaAs downconverting sigma-delta modulator and a silicon CMOS based digital signal processor which serves as an anti-alias filter and extracts the I-Q information from the IF output of the modulator.

The operation of the downconverting sigma-delta modulator is shown in Fig 2.3.2. The loop first translates the incoming signal to a low IF (nominally 10 MHz). Second, the sigma-delta modulator samples and lowpass filters the translated signal, rejecting the sum component of the mixing process.

The proposed design of the demodulator was simulated on two different levels. The block diagram level behavior of the demodulator was simulated using Mathcad 5.0 and an internally developed C language program. Additionally, the GaAs sigma-delta modulator was simulated at the transistor level using SPICE3. Both these simulations were performed in the time domain to study the effects of nonlinear effects such as amplifier saturation, mixing, and quantization noise. We will elaborate on the proposed IC designs in the following sections.

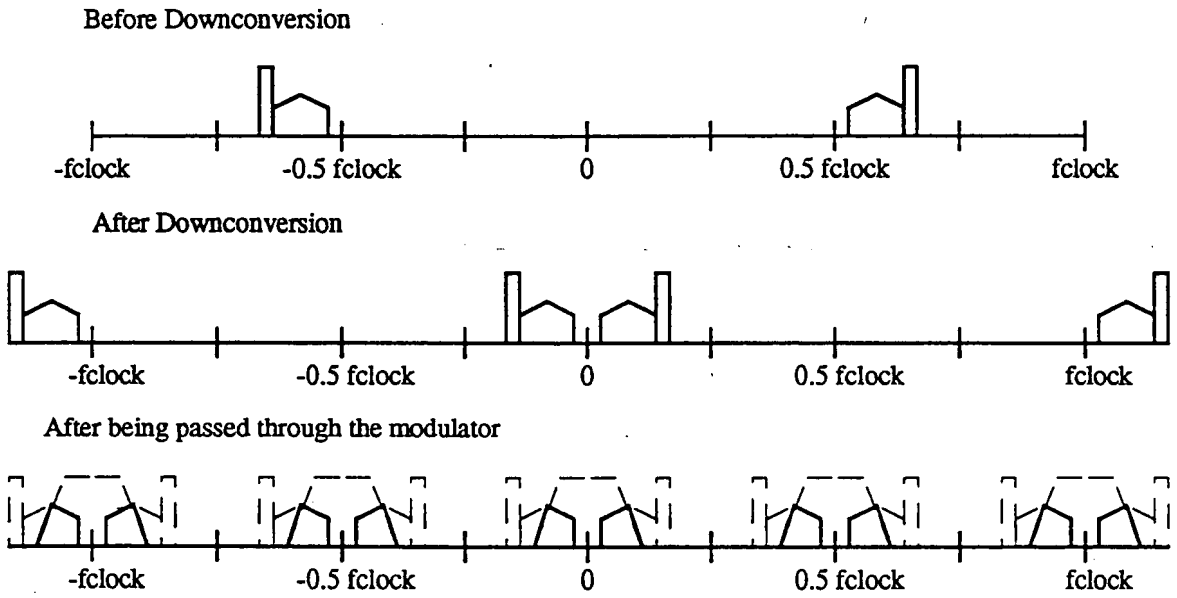


Fig. 2.3.2. Operation of the digital I-Q demodulator. The top diagram shows the spectrum of the incoming signal (which is offset in frequency from the clock frequency of the sigma-delta loop by the offset frequency - nominally 10 MHz). The middle diagram shows the effect of downconversion using half the sampling frequency. Finally, the effect of the sigma-delta modulator is shown in the bottom diagram; the lowpass response of the loop rejects all of the high frequency components.

3.3. Modulator Design

The proposed modulator chip design uses TechnoConcepts' source-coupled FET logic (SCFL) approach. This logic approach is the most appropriate for mixed signal applications since the outputs are fully differential and the instantaneous power supply current is the same for logic "0" and logic "1" outputs. Thus current switching noise on the power supply buses is minimized along with the potential for crosstalk between signals. The use of differential outputs not only increases the noise margin over single-ended logic families but also tends to reject substrate noise and capacitive crosstalk noise as long as the true and complement outputs are routed along the same basic path. A schematic of a simple SCFL buffer appears in Fig. 3.3.1.

Referring to Fig. 2.3.1, the mixer function at the input of the modulator was implemented using a Gilbert multiplier type structure driven with a clock signal. Used in this manner, the mixer is actually a "chopper" which effectively multiplies the input by a "+1, -1, +1, ..." sequence that is equivalent to negating the gain polarity of the input amplifier on every half cycle of the clock. Since this occurs in synchrony with the phase switching of the double-sampled DAC outputs (implemented using a 2:1 MUX type structure), we expect that no significant undesired spurious products would result from this mixing operation. The unwanted mixing product (the sum of the carrier and clock frequencies) is rejected by the loop lowpass filter and therefore does not appear in the output.

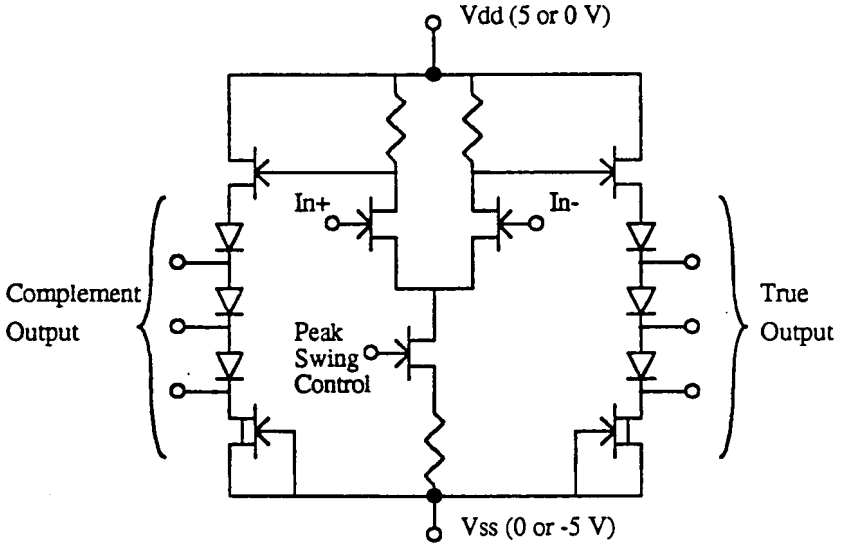


Fig. 3.3.1. Schematic of a simple SCFL buffer. The outputs occur at three separate voltage levels so that complex logic gates can be implemented while keeping all transistors in saturation. The peak swing control input is used to control the peak swing of the logic gate with a bandgap reference circuit.

As mentioned previously, in order to avoid the implementation of a large FIR filter within the modulator chip, we elected to maintain all of the output samples through the use of a time division demultiplexer. The demultiplexer is based upon network of cascaded 1:2 demultiplexers, which yields the lowest gate count implementation of this function. A simple block diagram of a 1:2 demultiplexer appears in Fig. 3.3.2. The circuit is based upon a master-slave D flip-flop architecture and automatically aligns the two outputs to the same phase of the clock.

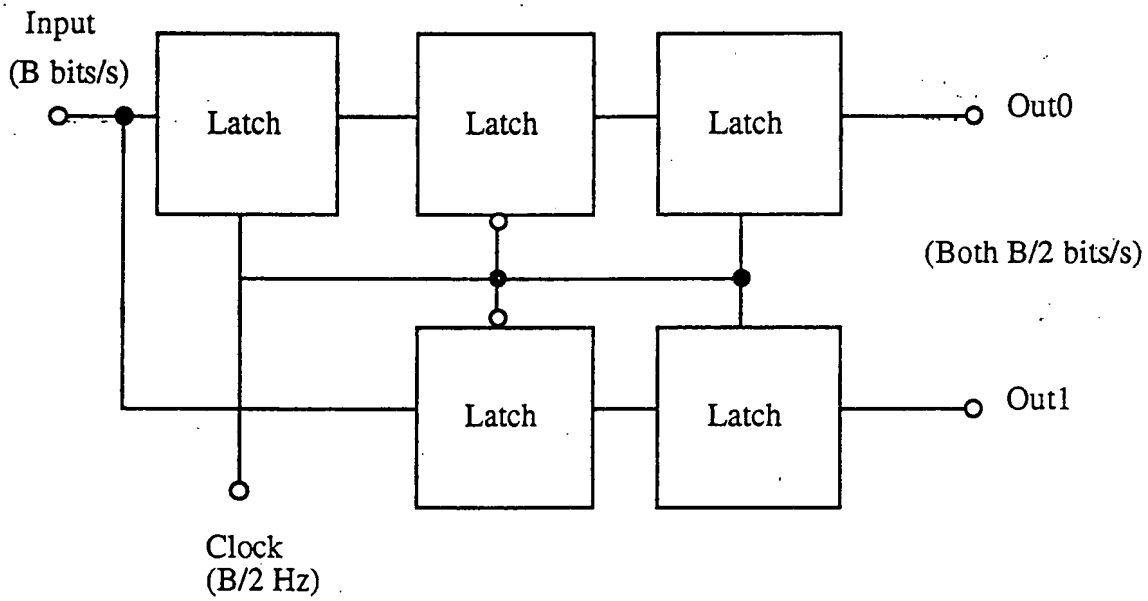


Fig. 3.3.2. Block diagram of a 1:2 demultiplexer. Based upon a master-slave D flip-flop architecture, the two outputs of the demultiplexer are synchronously aligned to the same clock phase.

A simulation of the sigma-delta modulator (without the 2:32 demultiplexer) appears in Appendix A. In this simulation, the outputs of the two 1-bit A/D circuits have been resistively summed and passed through a single pole RC filter in order to reject the quantization noise.

Our initial estimate of the power dissipation for this chip breaks down as follows:

Block Name	No. of Physical Gates ("Tails") per Block	Power Dissipation per Gate	Total Power Dissipation
Sigma-Delta Modulator	-	-	50 mW
2 GHz Clock Driver	1	41 mW	41 mW
"Zeroth" Stage of DEMUX	1	5 mW	5 mW
First Stage of DEMUX	7×2	5 mW	60 mW
Second Stage of DEMUX	7×4	2.5 mW	60 mW
Third Stage of DEMUX	7×8	1.25 mW	60 mW
Fourth Stage of DEMUX	7×16	0.5 mW	60 mW
Total	-	-	**330 mW**

3.4. Decimator/Demodulator Design

As mentioned earlier in this report, the proposed decimator/demodulator chip is envisioned as a conventional CMOS design, operating from a 3.3 volt power supply. In order to minimize the power dissipation of the GaAs chip (which would normally drive ECL or PECL levels into 50Ω), a specialized current interface was developed. A simplified schematic diagram of this current interface is shown in Fig. 3.4.1.

Although a complete preliminary design of this chip has not yet been completed, a design of the most critical portion (the 320-tap FIR filter) has been designed and simulated. The FIR filter, designed using the Remez exchange algorithm, exhibits about 90 dB of rejection in the stopband. However, when the coefficients are rounded off to a fixed resolution of 18 bits, the stopband rejection degrades to approximately 84 dB. A complete analysis of this 320-tap FIR appears in Appendix B.

The output of the FIR filter is a 14 bit sequence representing the IF signal modulated with the baseband information to be extracted. The functions following the filter are relatively simple in comparison. The sequence generated by the "I-Q sequence generator" ("1, 0, -1, 0" for cosine and "0, 1, 0, -1" for sine) is easily generated using a switching network. Note that I and Q sequences never simultaneously take on a non-zero value. The

interpolator is currently envisioned as a zeroth or first-order circuit and therefore would involve at most a single addition and scaling operation (albeit at 14 bit resolution). Note that the image rejection filter that is normally placed after the I-Q mixing operation is omitted; in the current design; this function is being performed off-chip. Our current estimate for the power dissipation of this IC (which we estimate to be approximately 10,000 gates in complexity is approximately 300-500 mW.

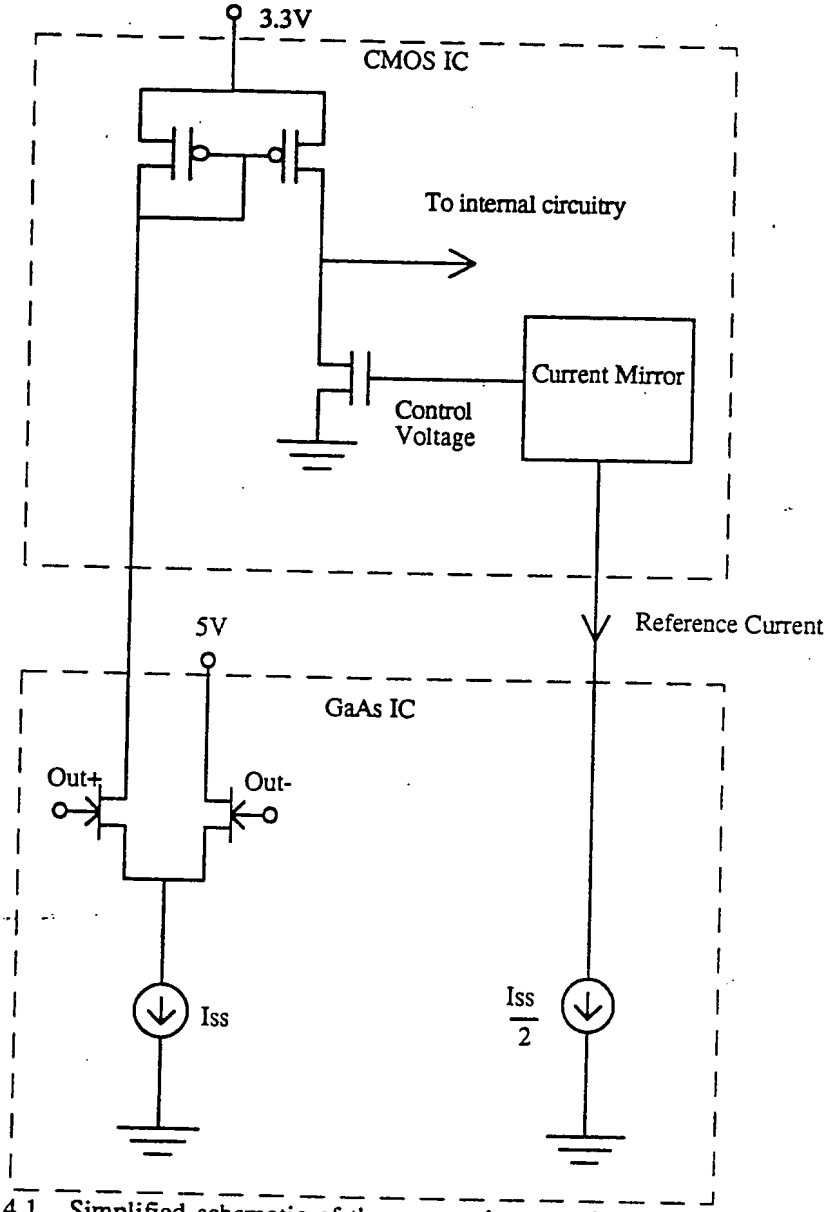


Fig. 3.4.1. Simplified schematic of the proposed current interface between the GaAs modulator and the silicon decimator/demodulator chip.

3.5. *Analysis of the Digital I-Q Demodulator Design*

As mentioned previously, the design of the digital I-Q demodulator was simulated numerically in order to verify its performance in light of non-linear effects which have the

potential of degrading its performance. This was done initially using Mathcad 5.0, implementing the trapezoidal approximation to integration with a step size equal to 1/20 of a clock period. However, in the course of running these simulations, it was discovered that the "numerical" noise associated with the discrete time simulation was such that 14-bit resolution could not be achieved. Thus, a C language program was written and longer simulations were performed (using both a finer time step and longer period of time). The simulations demonstrated a dynamic range of 14 bits; however, a small amount of gain flattening seemed to occur at "6-7 bits down" (1/64 - 1/128) from full scale amplitude. The results of these simulations are shown in Appendix C.

3.6. Conclusions

In this study, the preliminary conceptual design for a complete digital sigma-delta I-Q demodulator was developed. This design is based upon a two chip set which is comprised of a GaAs sigma-delta modulator and a silicon CMOS digital signal processor. A preliminary transistor-level design of the modulator was developed. A logical design for the 320-tap FIR filter was also developed; however, some minor development work in the logical implementation of the (non-integer) data rate reduction circuit as well as the I-Q numerical mixer must be completed. The next section will present a plan for completing this design level work as well as produce and characterize prototypes of the GaAs and silicon ASICs.

4. Proposed Follow-On Effort

4.1. Objectives of Follow-On Effort

The objectives of the follow-on effort for this project are:

- To complete an end-to-end simulation of the entire I-Q modulator with representative signals in order to establish the performance of the GaAs/silicon chip combination.
- To complete the detailed logical design for the silicon CMOS decimator/demodulator chip.
- To review and refine the design of the GaAs sigma-delta modulator chip.
- To complete the simulation, layout, and verification of the two designs.
- To verify the performance of the two ICs.

4.2. Work Plan and Proposed Milestones

In order to accomplish the aforementioned objectives, the work plan is organized as outlined in Table 4.2.1. The schedule assumes a nominal start date of August 15, 1995 and a reasonably pessimistic scenario including wafer lot lead times of 12 weeks for GaAs and silicon (the best case lead times are 4 - 8 weeks). Time is, by far, the crucial element in this development. Thus the work plan is designed to run the two designs in parallel. It is important to note that, as shown in Table 4.2.2, even under slightly more optimistic scenarios, the availability dates of the chips will improve greatly. A PERT chart of the development effort appears in Appendix D.

Task	Estimated Start Date	Estimated Completion
Sigma-Delta Modulator (GaAs)		
Design (Mask 1a)	8/15/95	11/6/95
Fabrication (Mask 1a)	11/7/95	1/29/96
Charact. (Mask 1a)	1/30/96	2/19/96
Redesign (Mask 1b)	2/20/96	3/11/96
Fabrication (Mask 1b)	3/12/96	6/3/96
Charact. (Mask 1b)	6/4/96	6/24/96
Decimator-Demodulator (Silicon)		
Complete Analysis	7/24/95	8/11/95
Design (Mask 2a)	8/14/95	1/26/96
Fabrication (Mask 2a)	1/29/96	4/19/96
Charact. (Mask 2a)	4/22/96	5/10/96
Redesign (Mask 2b)	5/13/96	5/31/96
Fabrication (Mask 2b)	6/3/96	8/23/96
Charact. (Mask 2b)	8/26/96	9/13/96

Table 4.2.1. Chart of major milestones associated with the design and fabrication of the Sigma-Delta Modulator and Decimator-Demodulator chips.

Scenario	Acceleration (weeks)
Sigma-Delta Modulator (GaAs)	
Fabrication time reduced to 10 weeks	4
Fabrication time reduced to 8 weeks	8
Initial design time reduced to 8 weeks	4
Characterization and redesign time reduced to 4 weeks (total)	2
Redesign unnecessary	18
Decimator-Demodulator (Silicon)	
Fabrication time reduced to 10 weeks	4
Fabrication time reduced to 8 weeks	8
Characterization and redesign time reduced to 4 weeks (total)	2
Redesign unnecessary	18

Table 4.2.2. Estimated acceleration of chip availability under scenarios more optimistic than the assumptions of Table 4.2.1.

4.3. Cost of Development

The cost of developing the two integrated circuits is shown in Table 4.3.1. Note that the fabrication prices includes the cost of a full set of masks (which is between $35,000 and $40,000 per set). In that production runs would not require the creation of new mask sets, no inferences about production costs should be inferred from these numbers. Furthermore, the production pricing for wafers is also typically much less than those for engineering runs. Additionally, the pricing for silicon CMOS 0.6μm lots is currently fairly high; we expect that within a year (by which time production will take place) the lots prices for this technology will also drop dramatically. Currently, the primary vendors from which 0.6μm foundry services are available include: TSMC, VLSI Technology, AT&T, IBM, and Kawasaki. We expect others to come on board during the year. The GaAs process being used (Vitesse Semiconductor) is already among the least expensive of the processes available and we expect the situation to remain so. Should alternative vendors be necessary, TriQuint Semiconductor, Rockwell, or ITT should be considered.

GaAs Sigma-Delta Modulator

Item	Quantity	Price	Cost
Fabrication	2 lots	72,500	145,000
Labor	3,115 hours	60	186,900
Materials (Probe cards, packages, etc.)	-		5,130
Total			**$337,030**

Silicon Decimator-Demodulator Chip

Item	Quantity	Price	Cost
Fabrication	2 lots	90,000	180,000
Labor	3,200 hours	60	192,000
Materials (Probe cards, packages, etc.)	-		2,500
Total			**$374,500**

Table 4.3.1. Estimated cost of development for the GaAs and silicon chips being proposed.

4.4. Dominant Risk Factors and Risk Reduction Plan

As mentioned previously, the primary risks associated with this project are schedule related. However, there are some technical risks which bear some mentioning. The first of these risks is the resolution of the GaAs sigma-delta modulator to noise one or more noise phenomena. Because of the fully differential nature of SCFL, we expect that clock noise will not prove to be a major noise contributor. However, other noise phenomena such as 1/f noise and excessive quantization noise may be considerations. We believe that an increase in the order of the loop should combat any of these problems should they arise. For this reason, more than one design of the modulator will be implemented on the first mask (Mask 1a) for comparison purposes.

The second of these risks is the achievable maximum clock speed of either the silicon chip or the GaAs chip, or both in light of power dissipation requirements. We intend to use a 0.6 μm silicon CMOS process in order to minimize the speed-power product so that 125 MHz clock speeds can be achieved with minimal power. We have already demonstrated 150 ps clock delays in GaAs SCFL circuits; however, we intend to use extremely low-power library cells which have some clock speed risk associated with them due to the high sensitivity of delay with respect to fanout. Our risk minimization plan once again includes the development multiple designs for both chips so that a design considered to be a "fall back" (in this case, a high powered design with minimal speed risk) could be delivered to

meet system performance specifications. These multiple designs will be similar enough to one another so that several major design efforts will not have to be run in parallel.

It is important to note that these comprise far less risk than is normally borne by TechnoConcepts in its research oriented work. For example, the sigma-delta modulator being proposed in this project is less complex than the four-bit modulator already demonstrated and the silicon CMOS IC (at 10,000 - 20,000 gates) is a relatively low integration scale design compared to technology capabilities. We believe that TechnoConcepts has the experience and resources necessary to complete the development of the parts being proposed and bring this project to successful conclusion.

5. Appendix A

SPICE input file and simulation results for a double-sampled, downconverting sigma-delta modulator. For this simulation, a double-sideband, suppressed carrier input was used. The carrier frequency is equal to the clock frequency. The expected output is a 10 MHz sinusoid. The two 1-bit digital outputs have been resistively added and passed through a single pole RC filter in order to simulate the effect of a digital smoothing filter. See Section 3.3 for additional information.

```
** Translating Sigma-Delta Front End **
** This file contains information that is proprietary **
** to TechnoConcepts, Inc. **

.subckt front_end 5 6   7 8   9 10   15 16   4 3   19 1 2
** xin+, xin-=5,6  xq0+, xq0-=7,8  xq1+,x q1-=9,10 **
** yclk+, yclk-=15,16 **
** zout+, zout-= 4,3
** vlc=19 vdd=1 vss=2 **
rpu1 1 3 10k
rpu2 1 4 10k
cpu1 1 3 1000p
cpu2 1 4 1000p
zdr1ta 3 5 11 ENH1.0 10
zdr1tb 4 6 11 ENH1.0 10
zdr1tc 4 5 12 ENH1.0 10
zdr1td 3 6 12 ENH1.0 10
zdr1ba 11 15 17 ENH1.0 10
zdr1bb 12 16 17 ENH1.0 10
zcur1 17 19 20 ENH1.0 5.2
rcur1 20 2 4456
zdr2ta 4 7 13 ENH1.0 10
zdr2tb 3 8 13 ENH1.0 10
zdr2tc 4 9 14 ENH1.0 10
zdr2td 3 10 14 ENH1.0 10
zdr2ba 13 15 18 ENH1.0 10
zdr2bb 14 16 18 ENH1.0 10
zcur2 18 19 21 ENH1.0 5.2
rcur2 21 2 4456
.ends front_end

.subckt lshift 10 20 21 22 1 2
** input=10 **
** outputs w=20 x=21 y=22 **
** vdd=1 vss=2 **
zsf 1 10 20 ENH1.0 5.2
zd1 21 20 21 ENH1.0 5.2
zd2 22 21 22 ENH1.0 5.2
zpd 22 2 2 DEP1.8 5.2
.ends lshift

* cir2sub on df_a Tue Feb  7 16:44:15 1995
* path = /big/big1/cells/GaAs/df_a/df_a_dummy.spice
.subckt df_a 34 35 12 13 5 6 3 4 33 32 20 15 11 1 2
*@ Qvw                          34
*@ Qvwn                         35
*@ Qwx                          12
*@ Qwxn                         13
*@ Qxy                          5
*@ Qxyn                         6
*@ Qyy                          3
*@ Qyyn                         4
*@ x                            33
*@ xn                           32
```

```
*@ y                          20
*@ yn                         15
*@ vlc                        11
*@ Vdd                         1
*@ Vss                         2
* SPICE 3 Deck created from df_a_dummy.sim, tech=hgaas3
*
r1000  31 1 4056
* actual cell name res4000ohm_0
r1001  1 30 4056
* actual cell name res4000ohm_1
r1002  1 24 4056
* actual cell name res4000ohm_2
r1003  1 23 4056
* actual cell name res4000ohm_3
r1004  2 28 4456
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r1007  2 10 4456
* actual cell name res4800ohm_3
z1 3 2 2 DEP1.8 5.2
z3 3 5 3 ENH1.0 5.2
z4 4 6 4 ENH1.0 5.2
z2 4 2 2 DEP1.8 5.2
z5 7 2 2 DEP1.8 5.2
z7 9 11 10 ENH1.0 5.2
z8 5 12 5 ENH1.0 5.2
z9 6 13 6 ENH1.0 5.2
z10 14 15 9 ENH1.0 5.2
z11 9 11 16 ENH1.0 5.2
z12 7 17 7 ENH1.0 5.2
z13 8 18 8 ENH1.0 5.2
z14 19 20 9 ENH1.0 5.2
z15 21 11 22 ENH1.0 5.2
z16 23 13 14 ENH1.0 5.2
z17 24 12 14 ENH1.0 5.2
z18 23 25 19 ENH1.0 5.2
z19 24 26 19 ENH1.0 5.2
z20 17 26 17 ENH1.0 5.2
z21 18 25 18 ENH1.0 5.2
z22 27 20 21 ENH1.0 5.2
z23 21 11 28 ENH1.0 5.2
z24 29 15 21 ENH1.0 5.2
z25 30 25 27 ENH1.0 5.2
z26 31 26 27 ENH1.0 5.2
z27 30 32 29 ENH1.0 5.2
z28 31 33 29 ENH1.0 5.2
z29 12 34 12 ENH1.0 5.2
z30 13 35 13 ENH1.0 5.2
z31 26 36 26 ENH1.0 5.2
z32 25 37 25 ENH1.0 5.2
```
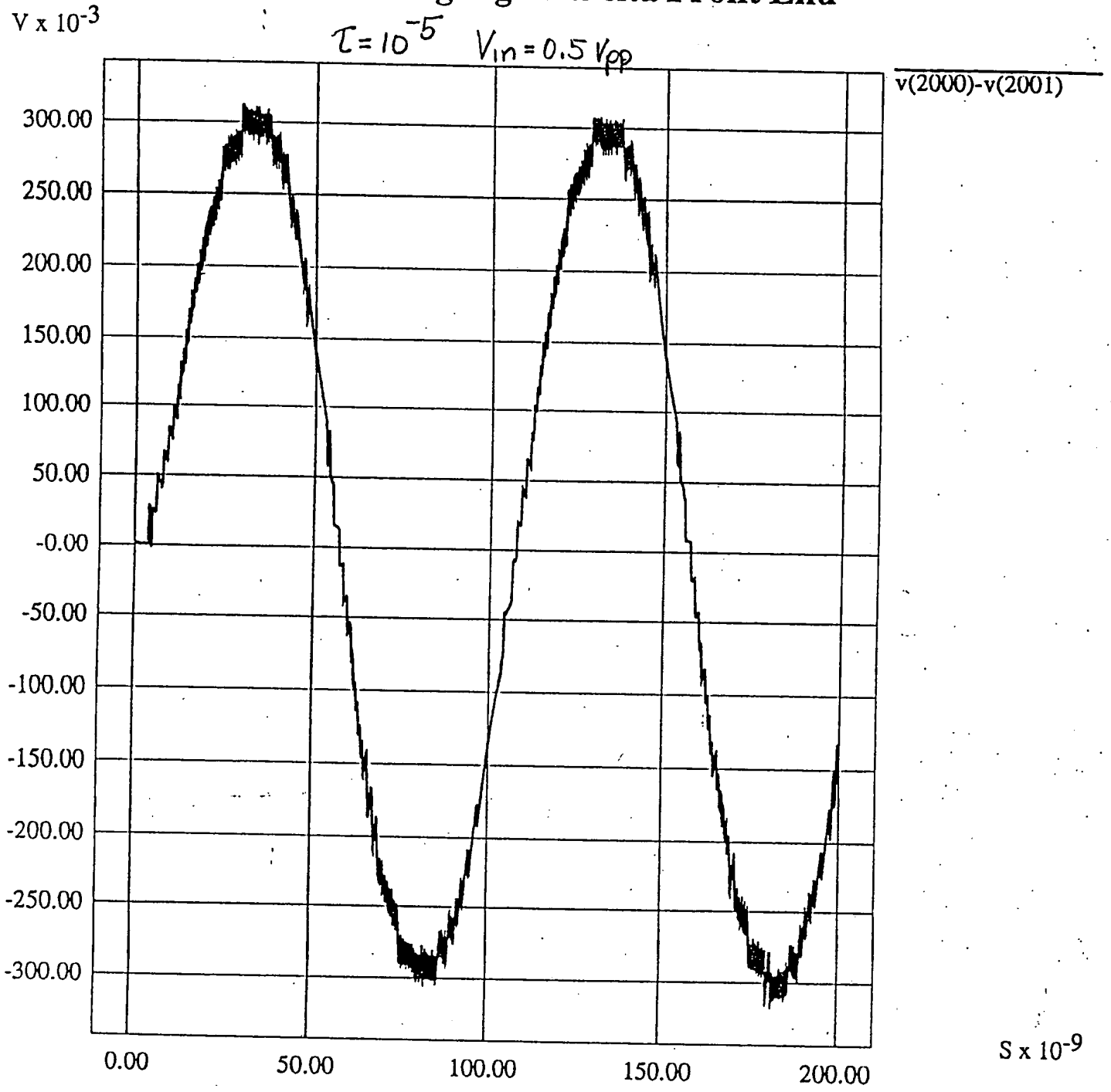

```
z33 1 24 35 ENH1.0 5.2
z34 1 31 37 ENH1.0 5.2
z35 1 23 34 ENH1.0 5.2
z36 1 30 36 ENH1.0 5.2
z6 8 2 2 DEP1.8 5.2
*
.ends df_a

.subckt op  5 6   12 11  14 13  16 15  18 17  8 1  2
** inputs = (5,6)
** outputs = (12,11) (14,13) (16,15) (18,17)
** voc = 12  vdd = 1  vss = 2
rpu1 1 3 8k
rpu2 1 4 8k
zdr1 3 5 7 ENH1.0 40
zdr2 4 6 7 ENH1.0 40
zcur1 7 8 9 ENH1.0 5.2
zcur2 7 8 10 ENH1.0 5.2
rcur1 9 2 4456
rcur2 10 2 4456
zsf1 1 3 11 ENH1.0 5.2
zls1a 13 11 13 ENH1.0 5.2
zls1b 15 13 15 ENH1.0 5.2
zls1c 17 15 17 ENH1.0 5.2
zpd1 17 2 2 DEP3.4 5.2
zsf2 1 4 12 ENH1.0 5.2
zls2a 14 12 14 ENH1.0 5.2
zls2b 16 14 16 ENH1.0 5.2
zls2c 18 16 18 ENH1.0 5.2
zpd2 18 2 2 DEP3.4 5.2
.ends op

* cir2sub on buf_a Mon Jan 16 12:59:44 1995
* path = /home/cells/GaAs/buf_a/buf_a_dummy.spice
.subckt buf_a 12 9 17 18 15 16 13 14 3 4 7 1 2
*@ x                    12
*@ xn                    9
*@ zvw                  17
*@ zvwn                 18
*@ zwx                  15
*@ zwxn                 16
*@ zxy                  13
*@ zxyn                 14
*@ zyy                   3
*@ zyyn                  4
*@ vlc                   7
*@ Vdd                   1
*@ Vss                   2
* SPICE 3 Deck created from buf_a_dummy.sim, tech=hgaas3
*
r1000  11 1 4056
* actual cell name res4000ohm_1
r1001  8 1 4056
* actual cell name res4000ohm_0
```

```
r1002  2 10 4456
* actual cell name res4800ohm_0
r1003  6 2 4456
* actual cell name res4800ohm_1
z1 3 2 2 DEP1.8 5.2
z3 5 7 6 ENH1.0 5.2
z4 8 9 5 ENH1.0 5.2
z5 5 7 10 ENH1.0 5.2
z6 11 12 5 ENH1.0 5.2
z7 3 13 3 ENH1.0 5.2
z8 4 14 4 ENH1.0 5.2
z9 13 15 13 ENH1.0 5.2
z10 14 16 14 ENH1.0 5.2
z11 15 17 15 ENH1.0 5.2
z12 1 8 17 ENH1.0 5.2
z13 1 11 18 ENH1.0 5.2
z14 16 18 16 ENH1.0 5.2
z2 4 2 2 DEP1.8 5.2
*
.ends buf_a

.subckt op_amp 1 2 10 11
egain 3 0 1 2 16384
rout 3 4 1g
sclamphi 4 6 4 0 smod2
vclamphi 6 0 .5
sclamplo 4 7 0 4 smod2
vclamplo 7 0 -.5
ebuff1 5 0 4 0 1
ebuff2 8 0 0 4 1
vls1 5 10 2.4
vls2 8 11 2.4
.ends op_amp
.model smod2 sw(vt=.5)

vdd 1 0 dc 0
vss 2 0 -5.2
vlc 20 0 -4.055
vmod 150 0 sin(0 1 10meg 0 0)
*vmod 150 0 dc 1
rmod 150 0 1g
vcar 151 0 sin(0 .125 2000meg 0 0)
rcar 151 0 1g
bin  100 0 v=v(150)*v(151)-2
*vinp 100 0 -2
vinn 101 0 -2
vclk  400 0 pulse(-3.9 -3.3 0 100p 100p 150p 500p)
vclkn 401 0 pulse(-3.3 -3.9 0 100p 100p 150p 500p)


xin 100 101 220 221 320 321 400 401 500 501 20 1 2 front_end
xls1 500 600 610 620 1 2 lshift
xls2 501 601 611 621 1 2 lshift
xop1 620 621 700 701 710 711 720 721 730 731 20 1 2 op
```

```
xop2 730 731 750 751 760 761 770 771 780 781 20 1 2 op
xop3 780 781 800 801 810 811 820 821 830 831 20 1 2 op
xop4 830 831 850 851 860 861 870 871 880 881 20 1 2 op
*xopamp 610 611 810 811 op_amp
xbuf 880 881 900 901 910 911 920 921 930 931  20 1 2 buf_a
xdf1 200 201 210 211 220 221 230 231 910 911 400 401 20 1 2 df_a
xdf2 300 301 310 311 320 321 330 331 910 911 401 400 20 1 2 df_a
rfilt1a 200 2000 50k
rfilt1b 300 2000 50k
cfilt1 2000 0 300f
rfilt2a 201 2001 50k
rfilt2b 301 2001 50k
cfilt2 2001 0 300f

.tran 40p 200n

** HGaAs3 Models from UCSB **
** Includes additions from R. Hickling to model special long fets **

*  L=0.8um  W=1um  depletion mode mesfet (1.0um as bloated)
.model DEP1.0 nmf(vto=-1.1 beta=2.27e-4 lambda=0.065 alpha=2.63
+ b=0.89 rs=430 rd=430 is=2e-17 cgs=1.4ff cgd=0.08ff pb=0.8)

*  L=1.6um  W=1um  depletion mode mesfet (1.8um as bloated)
.model DEP1.8 nmf(vto=-0.91 beta=1.45e-4 lambda=0.054 alpha=2.48
+ b=0.19 rs=875 rd=875 is=2e-17 cgs=2.8ff cgd=0.16ff)

*  L=3.2um  W=1um  depletion mode mesfet (3.4um as bloated)
.model DEP3.4 nmf(vto=-0.91 beta=7.25e-5 lambda=0.054 alpha=2.48
+ b=0.19 rs=1750 rd=1750 is=2e-17 cgs=5.6ff cgd=0.32ff)

*  Special FET added to accommodate the Dcap **
*  L=98.4um  W=1um depletion mode mesfet (98.6um as bloated)
.model DEP98.6 nmf(vto=-0.91 beta=2.36e-6 lambda=0.054 alpha=2.48
+ b=0.19 rs=53812 rd=53812 is=2e-17 cgs=172.2ff cgd=9.84ff)

*  L=0.8um w=1um  enhancement mode mesfet (1.0um as bloated)
.model ENH1.0 nmf(vto=0.024 beta=1.22e-4 lambda=0.35 alpha=5.21
+ b=5.2e-3 rs=460 rd=460 is=2e-17 cgs=0.5ff cgd=0.1ff pb=0.9)

.END
```

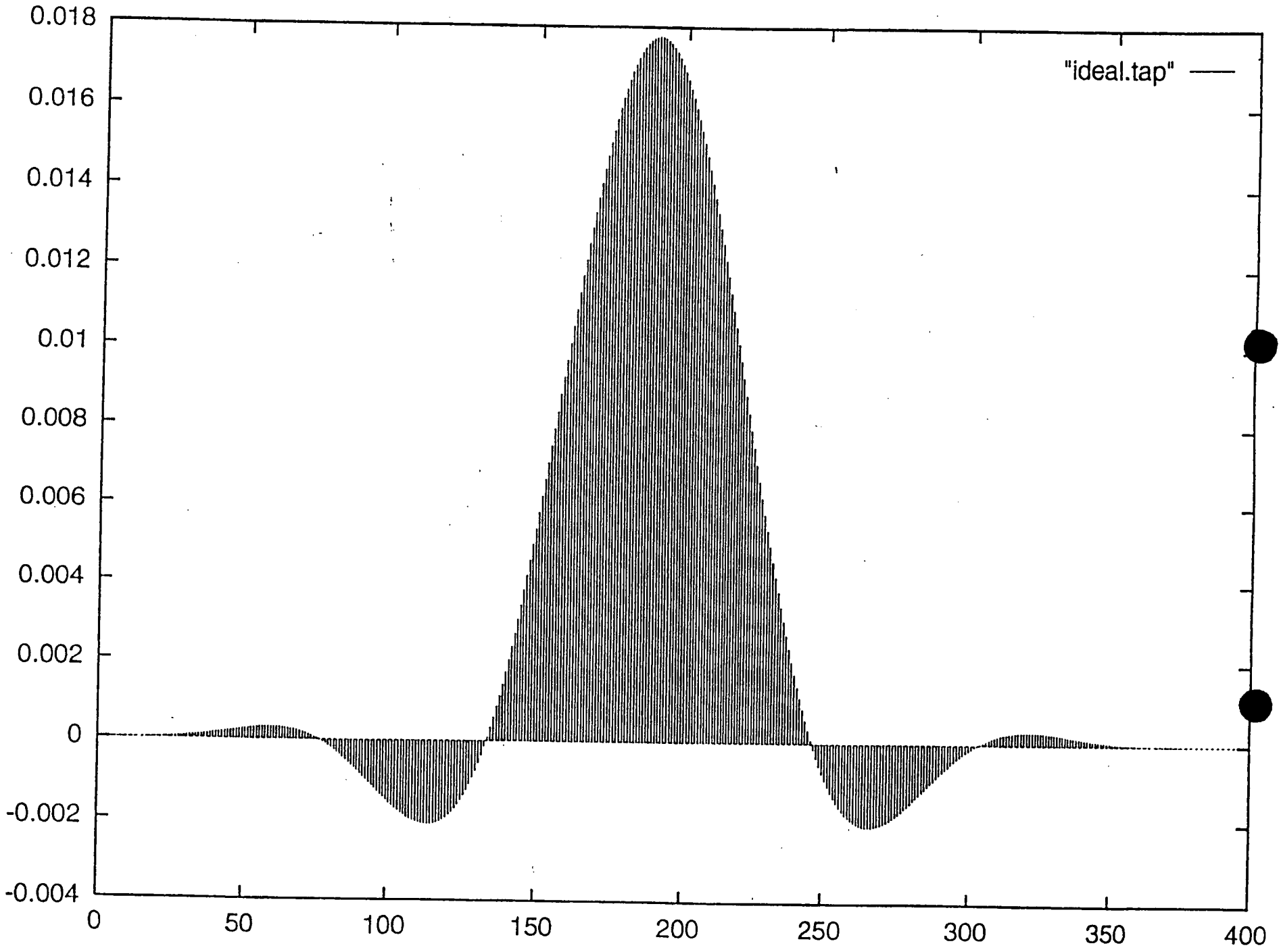
** Translating Sigma-Delta Front End **

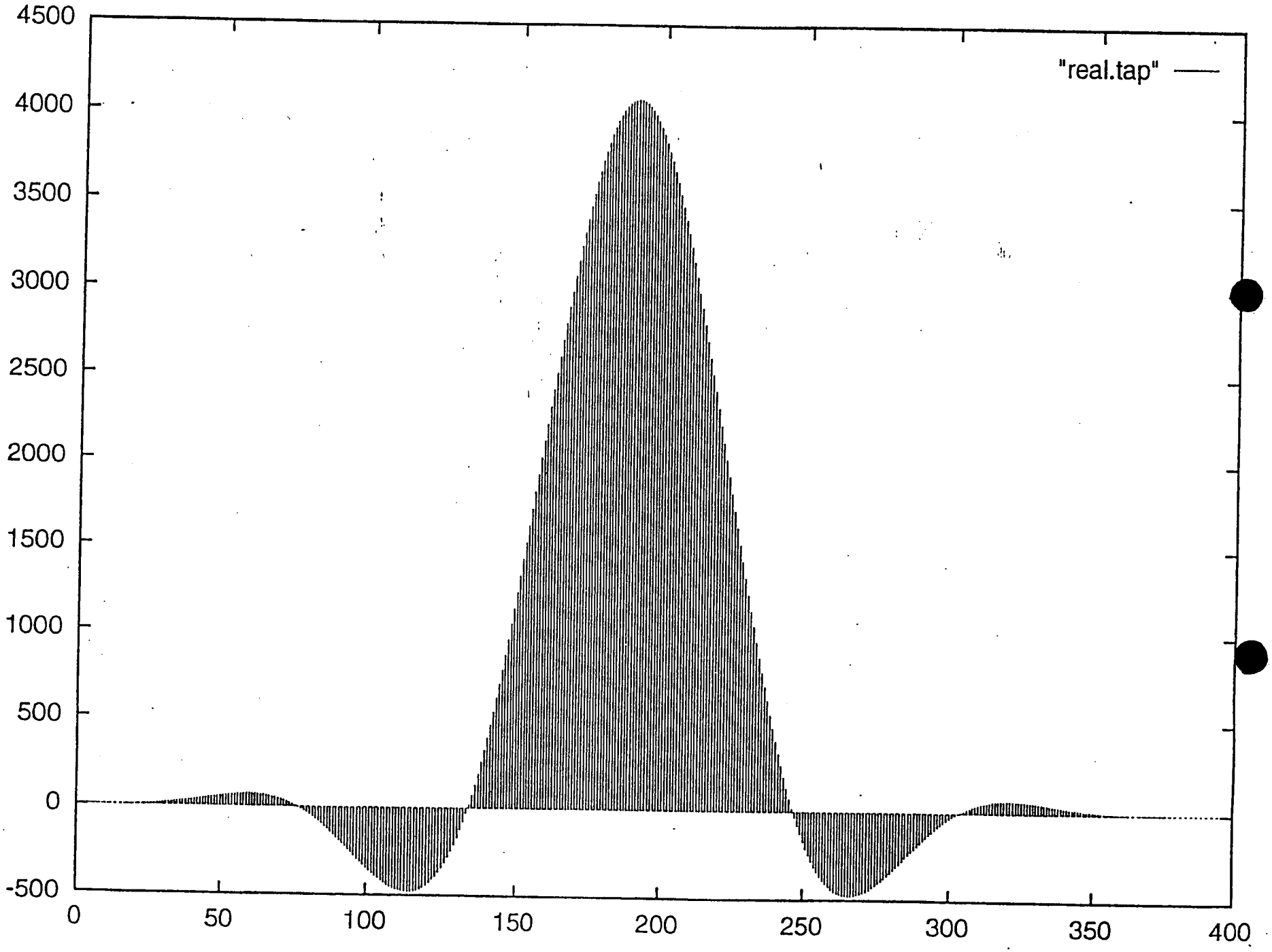


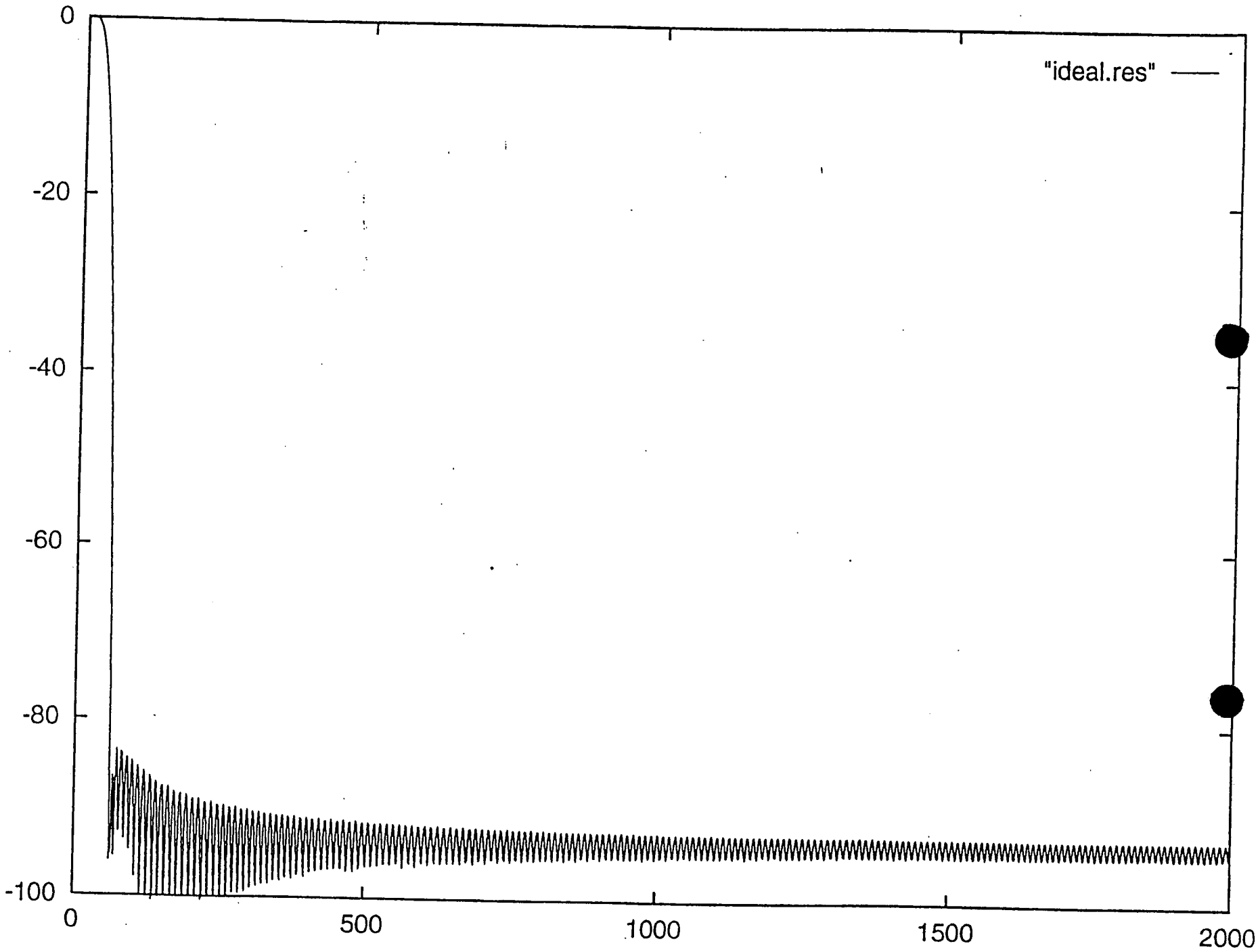
6. Appendix B

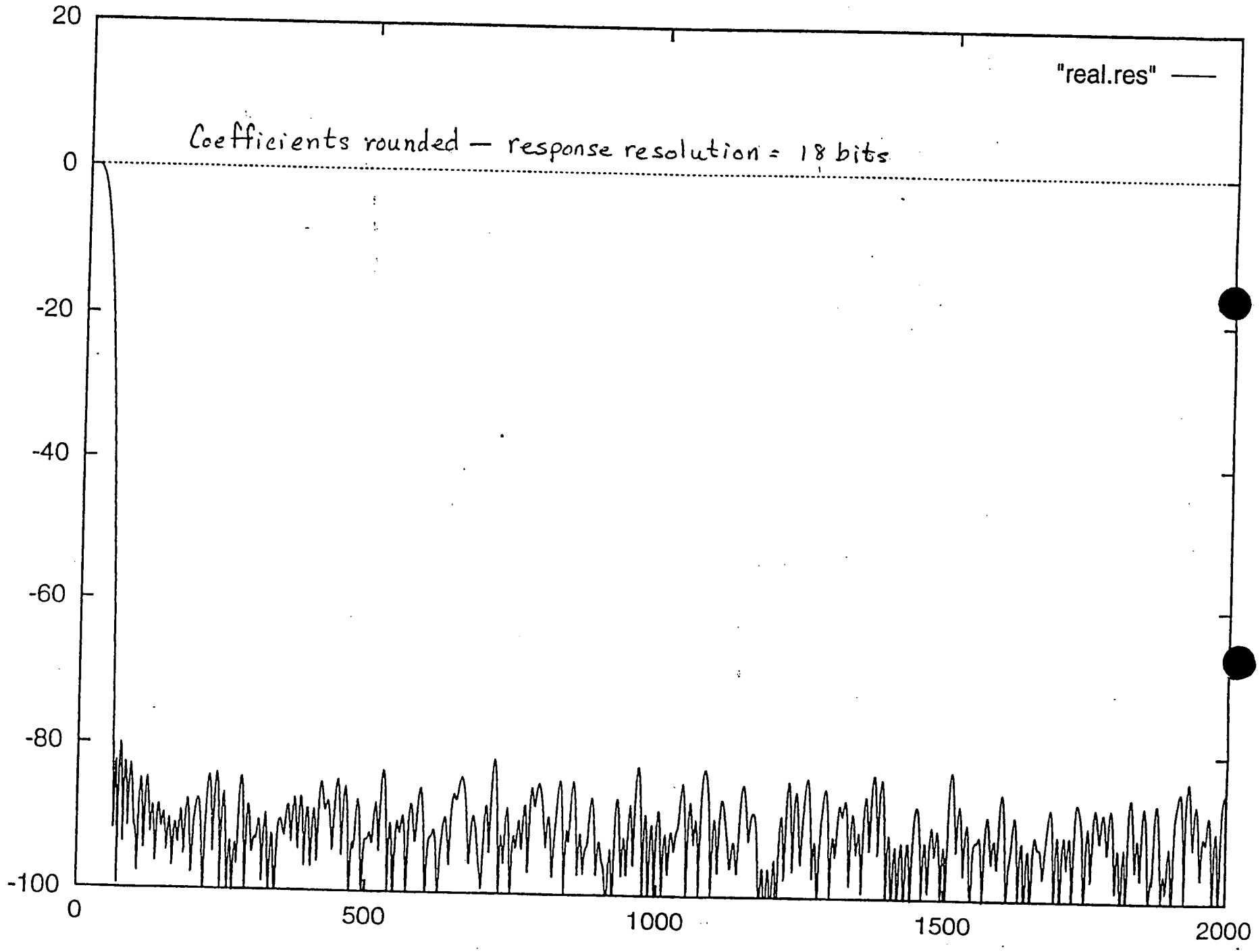
Frequency response for a 320-tap FIR filter designed using the Remez exchange algorithm. The five plots to follow (in order) are:

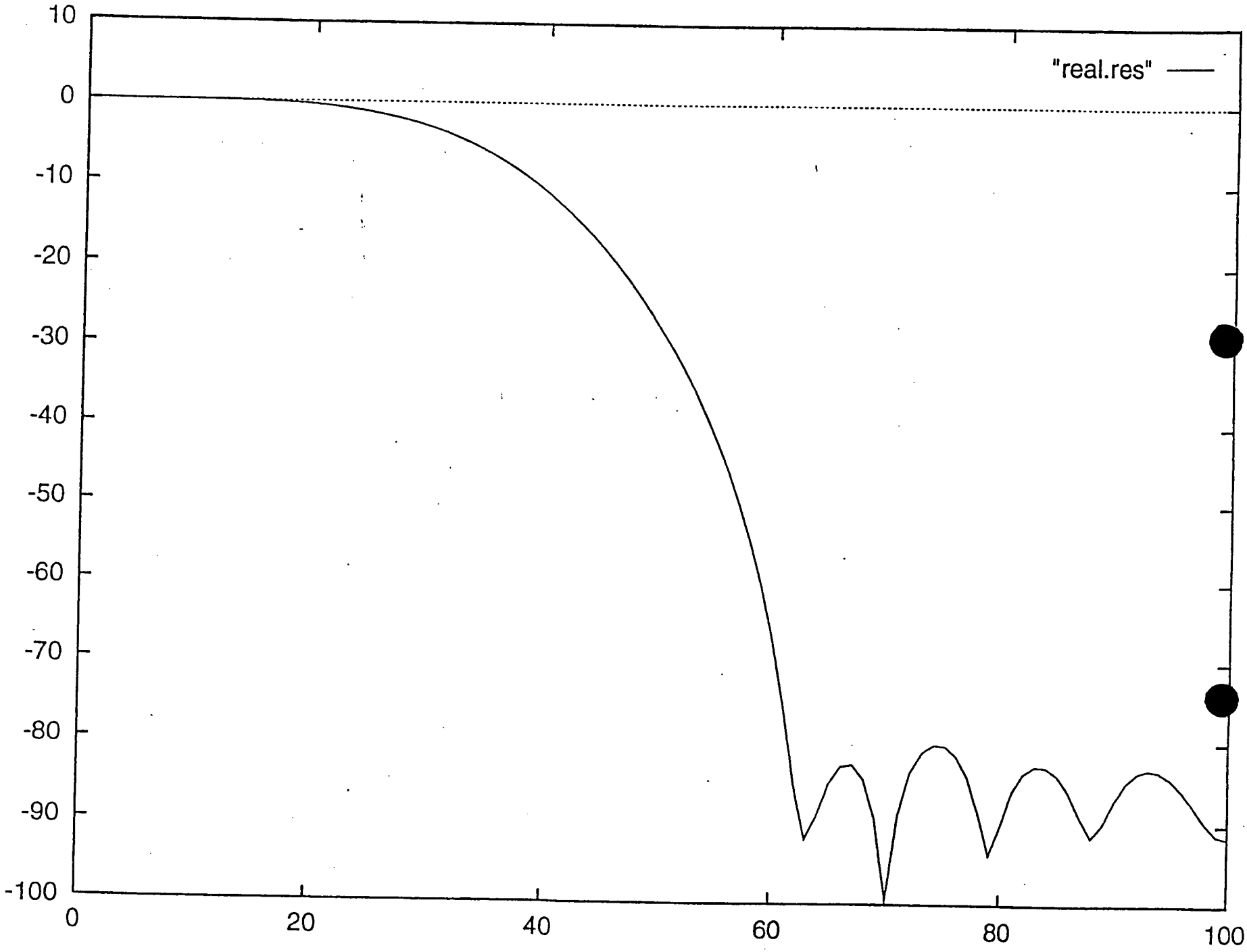
- The ideal time domain response
- The time domain response rounded to 18 bits resolution
- The ideal frequency response
- The frequency response of the filter with coefficients rounded to 18 bits resolution ("Real Response")
- The Expanded view of the "Real Response" showing the transition band in the frequency response.


"ideal.tap"
0.018
0.016
0.014
0.012
0.01
0.008
0.006
0.004
0.002
0
-0.002
-0.004
0
50
100
150
200
250
300
350
400


"real.tap"
4500
4000
3500
3000
2500
2000
1500
1000
500
0
-500
0
50
100
150
200
250
300
350
400


"ideal.res"
0
-20
-40
-60
-80
-100
0
500
1000
1500
2000


"real.res"
Coefficients rounded — response resolution = 18 bits
20
0
-20
-40
-60
-80
-100
0
500
1000
1500
2000


"real.res"
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
20
40
60
80
100

7. Appendix C

Numerical simulation of the sigma-delta in response to a double sideband suppressed carrier input signal. In the Mathcad 5.0 simulation, only the modulator was considered. In the C language simulations, the modulator as well as the 2:32 demultiplexer and 320-tap FIR filter was considered. The documents to follow are:

- A Mathcad 5.0 simulation of the sigma-delta modulator
- A series of plots showing the FFT of the response of a series of C language simulations (from a 1 volt amplitude input signal down to a 1/16384 volt amplitude input signal) implementing the same code as the Mathcad simulation with the exception of the smaller time step and long simulation times.
- A plot of the output amplitude of the 10 MHz signal versus the input amplitude of the double sideband-suppressed carrier input over the 14 bits of dynamic range simulated.

These plots demonstrates a 14-bit dynamic range wherein the signal is at least 6 dB above the noise floor. However, in these simulations a flattening of the signal sensitivity was observed around 1/64 to 1/128 of full scale amplitude.

Time domain simulation of a downconverting sigma-delta converter (w/ one bit quantizers)

$fclk := 1890 \cdot 10^{6}$ clock frequency

$ts := \frac{1}{40 \cdot fclk}$ time step

$tmax := 200 \cdot 10^{-9}$ length of simulation

$npp := \frac{tmax}{ts}$ number of desired time points in simulation

$Npp := ceil\left(\frac{\log(npp)}{\log(2)}\right)$ Npp used to make simulation 2^Npp points long

$Nmax := 2^{Npp}$ Actual number of points in simulation $Nmax = 1.638 \cdot 10^{4}$

Sigma-delta parameters

$opgain := 16384$ Op amp gain

$oprail := 1$ Op amp rails = +/- oprail

$\tau int := 10^{-4}$ Time constant of integrator pole

$k := .5$ Feedback attenuation factor (k<1). The summing node is effectively driven by the signal x=(1-k)*vin-k*vout

$dacfs := 1$ Dac active range = +/- dacfs

$i := 0 .. Nmax - 1$

$t_i := ts \cdot i$ $t_{Nmax-1} = 2.167 \cdot 10^{-7}$

$ck_i := if\left(\sin\left(2 \cdot \pi \cdot fclk \cdot t_i\right) > 0, 1, -1\right)$ Clock full scale amplitude=.01

$input\_amplitude := 1$ $fmod := 10 \cdot 10^{6}$ $fcarrier := fclk$

Above parameters are used to define the input signal (a DSB-SC waveform)

$vin_i := input\_amplitude \cdot \left(\cos\left(2 \cdot \pi \cdot fmod \cdot t_i\right) \cdot \sin\left(2 \cdot \pi \cdot fcarrier \cdot t_i\right)\right)$

$\alpha := 2 \cdot \frac{\tau int}{ts}$ $\alpha = 1.512 \cdot 10^{7}$

$j := 2 .. Nmax - 1$

$$\begin{bmatrix} x_0 \\ lpf_0 \\ y0_0 \\ y1_0 \end{bmatrix} := \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad \begin{bmatrix} x_1 \\ lpf_1 \\ y0_1 \\ y1_1 \end{bmatrix} := \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} x_j \\ lpf_j \\ y0_j \\ y1_j \end{bmatrix} := \begin{bmatrix} (1-k)\cdot ck_{j-1}\cdot vin_{j-1} - k\cdot if\left(ck_{j-1}>0, y0_{j-1}, y1_{j-1}\right) \\ \left[\frac{opgain}{1+2\cdot\alpha}\cdot\left(x_{j-1}\right) + \frac{opgain}{1+2\cdot\alpha}\cdot\left(x_{j-2}\right)\right] - \frac{1-2\cdot\alpha}{1+2\cdot\alpha}\cdot lpf_{j-1} \\ if\left[\left(ck_{j-1}>0\right)\cdot\left(ck_{j-2}\le 0\right), if\left(lpf_{j-1}>0, dacfs, -dacfs\right), y0_{j-1}\right] \\ if\left[\left(ck_{j-1}<0\right)\cdot\left(ck_{j-2}\ge 0\right), if\left(lpf_{j-1}>0, dacfs, -dacfs\right), y1_{j-1}\right] \end{bmatrix}$$

$$\tau := \frac{1}{2\cdot\pi\cdot 10\cdot 10^6} \qquad h := READPRN(h) \qquad htap := rows(h)$$

$$y_i := \frac{y0_i + y1_i}{2} \qquad z_0 := 0 \qquad z_1 := 0 \qquad z_j := \frac{y_j + y_{j-1}}{1+2\cdot\frac{\tau}{ts}} - \frac{1-2\cdot\frac{\tau}{ts}}{1+2\cdot\frac{\tau}{ts}}\cdot z_{j-1}$$

$$ysamp_0 := 0 \qquad ysamp_1 := 0 \qquad zz_0 := 0 \qquad zz_1 := 0$$

$$ysamp_j := if\left[\left(ck_{j-1}\cdot ck_{j-2}\right)<0, y_j, ysamp_{j-1}\right] \qquad nclk := \frac{1}{2\cdot fclk\cdot ts}$$

$$zz_j := \sum_{jj=0}^{htap-1} if\left(j - nclk\cdot jj>0, h_{htap-jj-1}\cdot ysamp_{j-nclk\cdot jj}, 0\right)$$

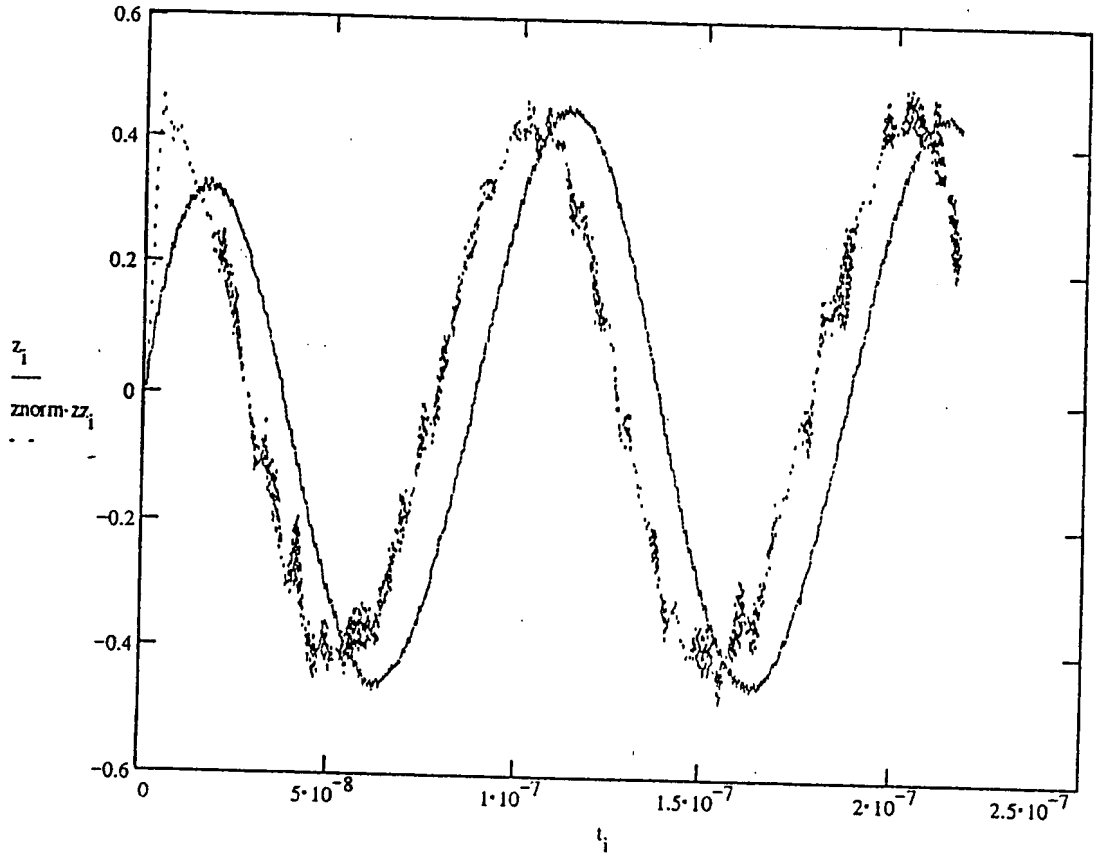
$$Z := FFT(z) \qquad ZZ := FFT(zz)$$

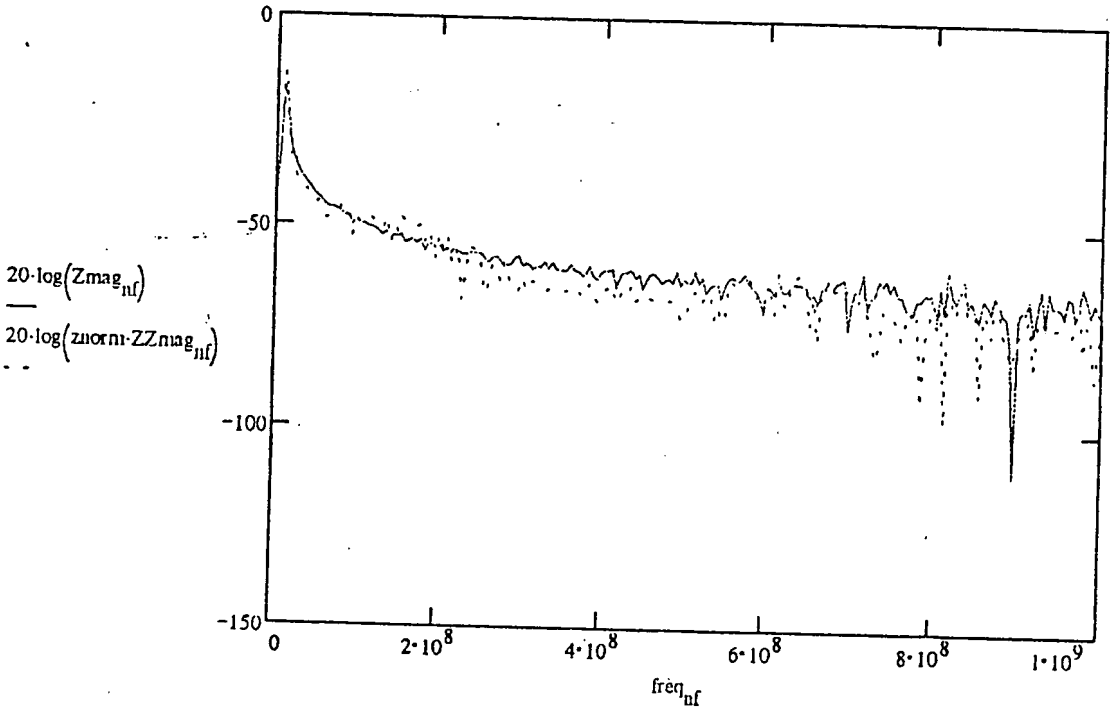
$$Y := FFT(y)$$

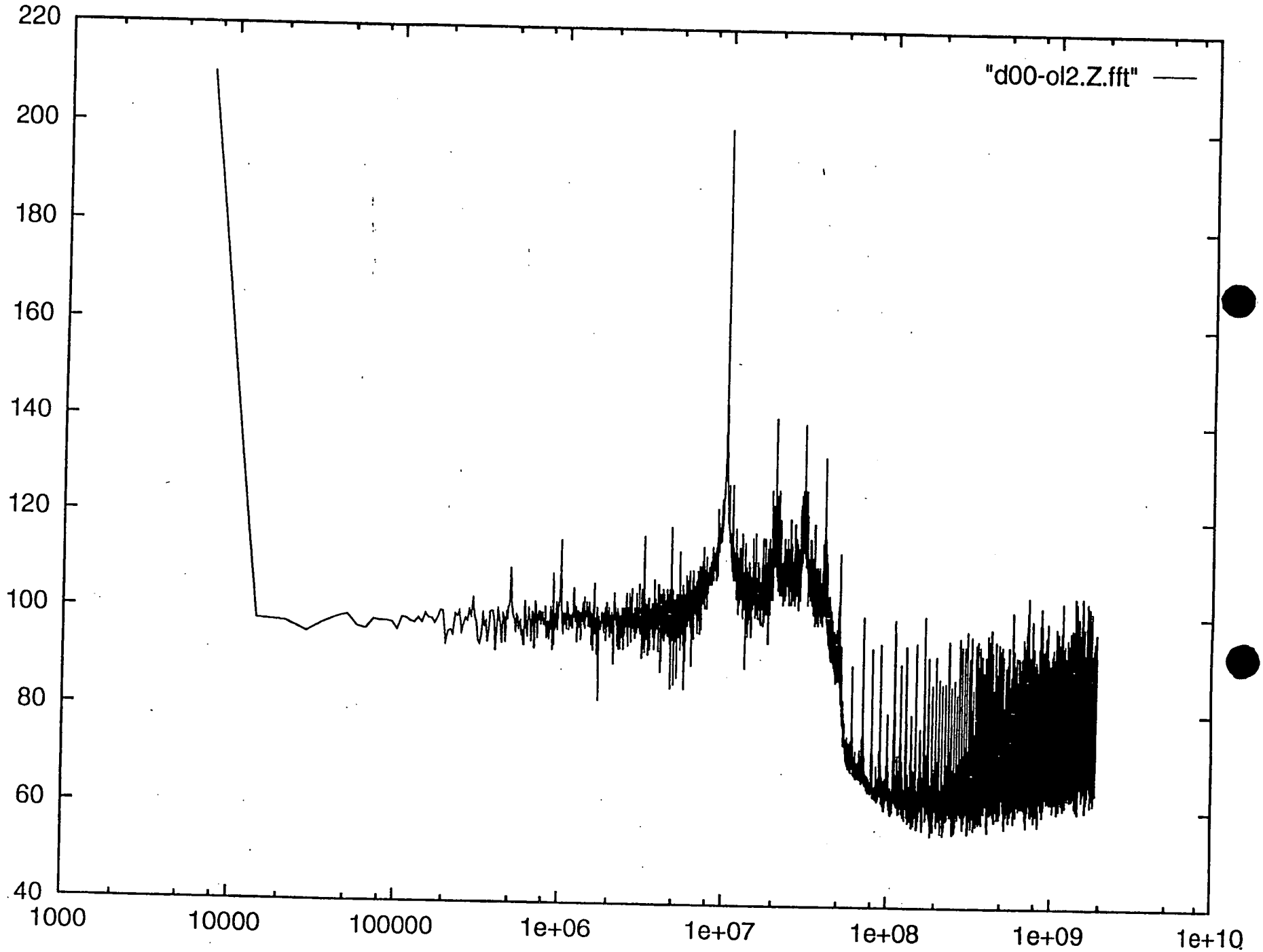
$$nfreq := rows(Z) \qquad nfreq = 8.193\cdot 10^3 \qquad nmod := floor((2\cdot ts\cdot nfreq)\cdot fmod + 0.5)$$

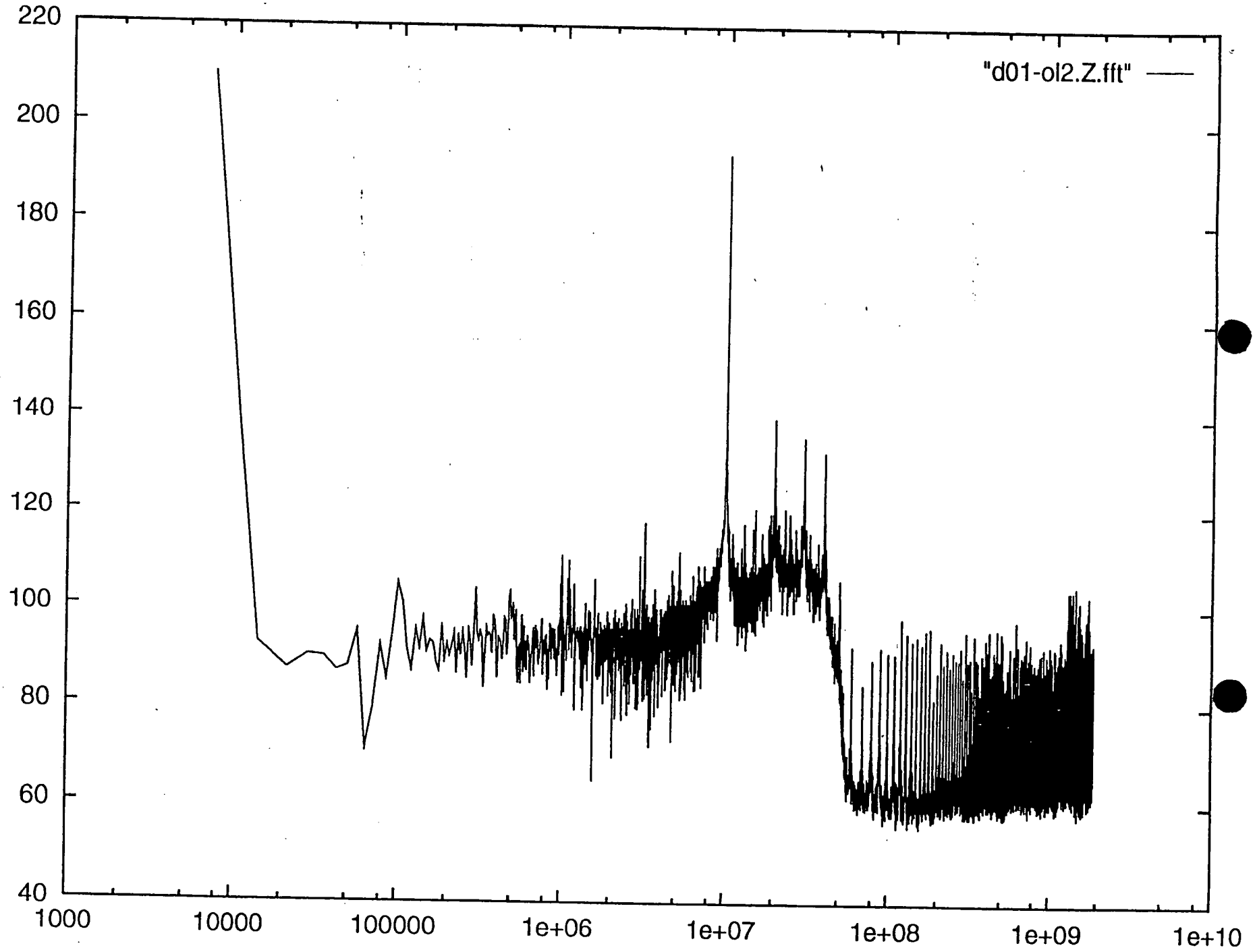
$$nf := 0..nfreq-1$$

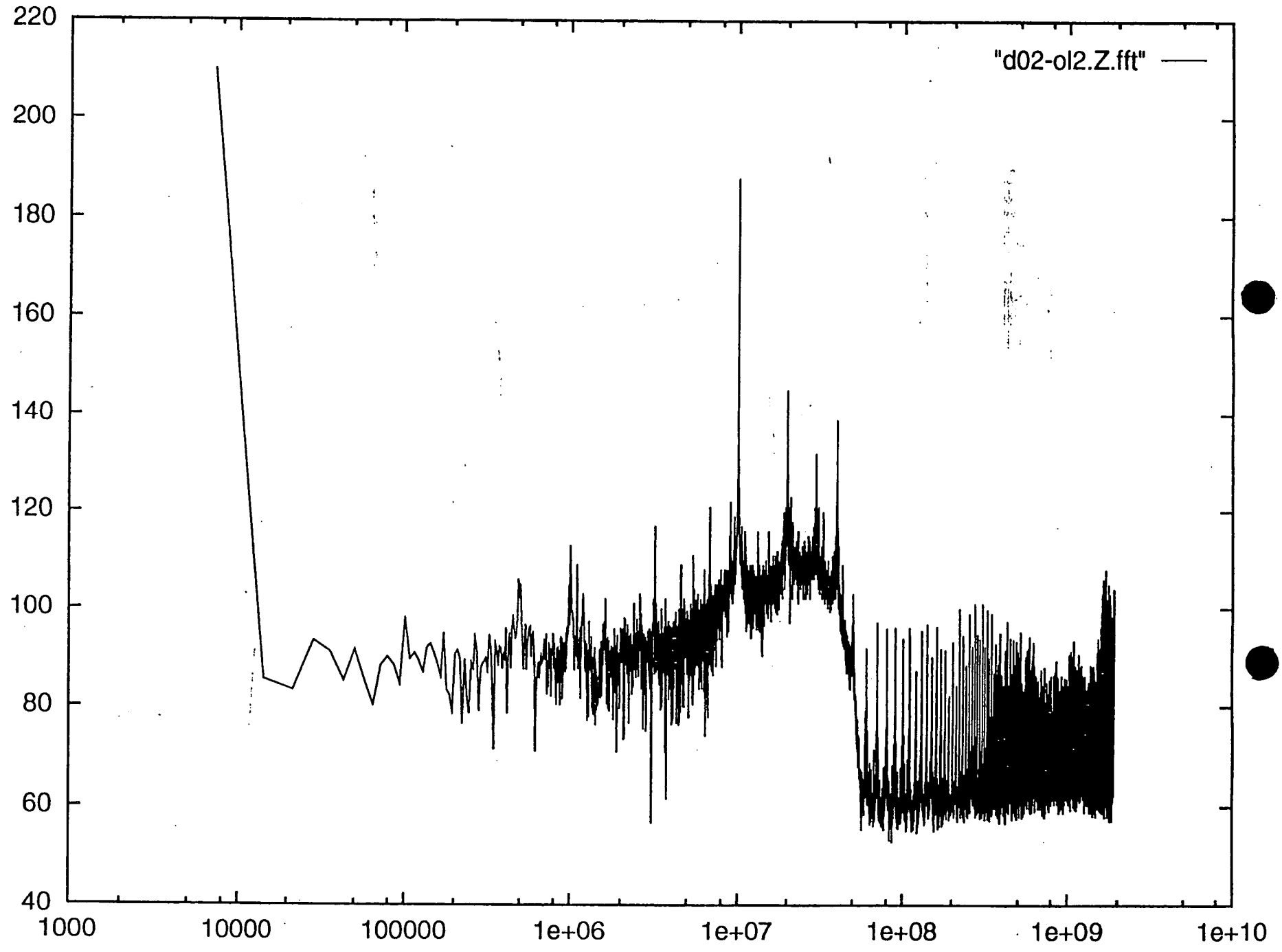
$$freq_{nf} := \frac{nf}{2\cdot ts\cdot nfreq} \qquad Zmag_{nf} := \left|Z_{nf}\right| + 10^{-200} \qquad ZZmag_{nf} := \left|ZZ_{nf}\right| + 10^{-200} \qquad znorm := \frac{Zmag_{nmod}}{ZZmag_{nmod}}$$


0.6
0.4
0.2
0
−0.2
−0.4
−0.6
0
5·10^−8
1·10^−7
1.5·10^−7
2·10^−7
2.5·10^−7
t_i
z_i
znorm·zz_i


0
−50
−100
−150
0
2·10^8
4·10^8
6·10^8
8·10^8
1·10^9
freq_nf
20·log(Zmag_nf)
20·log(znorm·ZZmag_nf)


"d00-ol2.Z.fft"
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10


"d01-ol2.Z.fft"
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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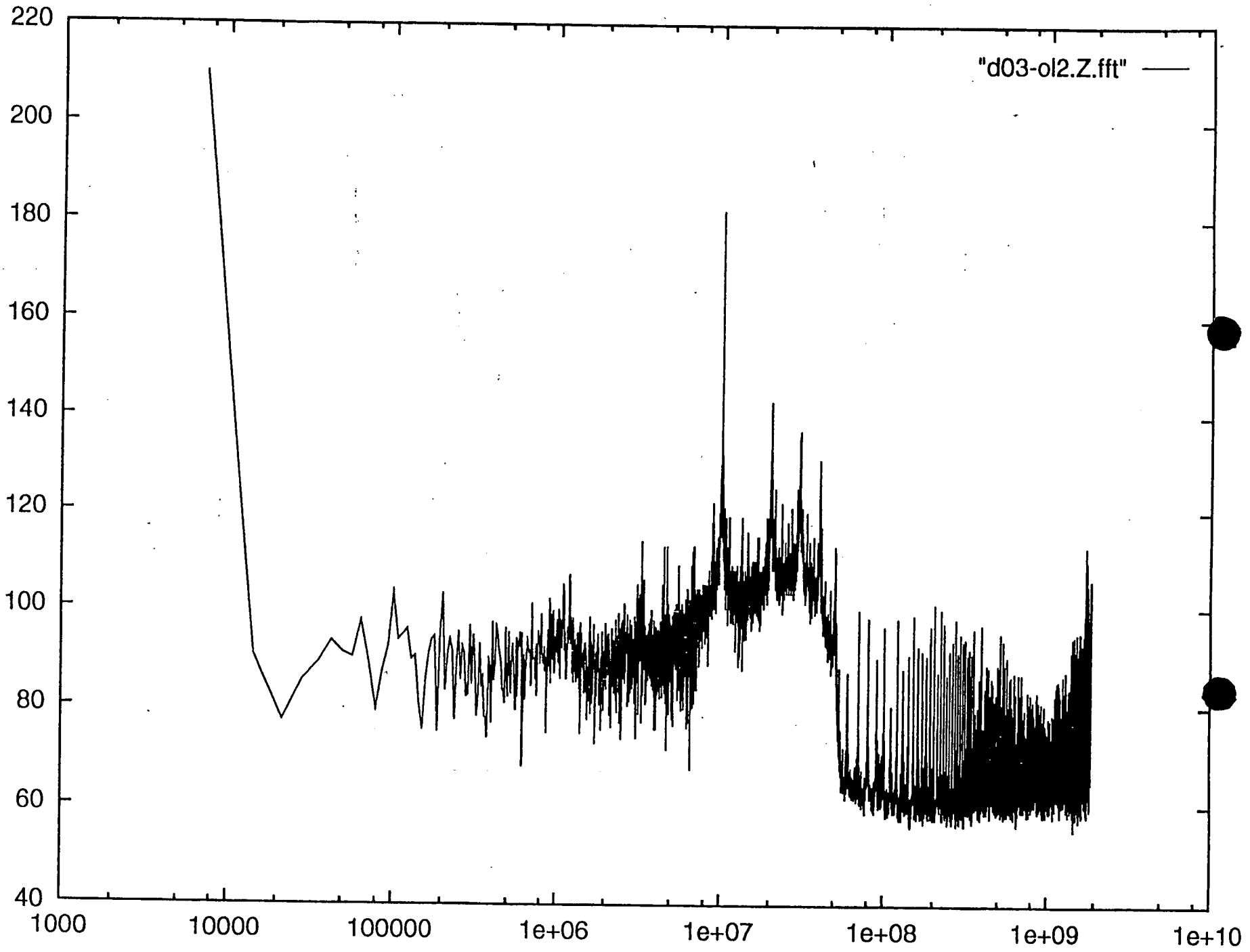
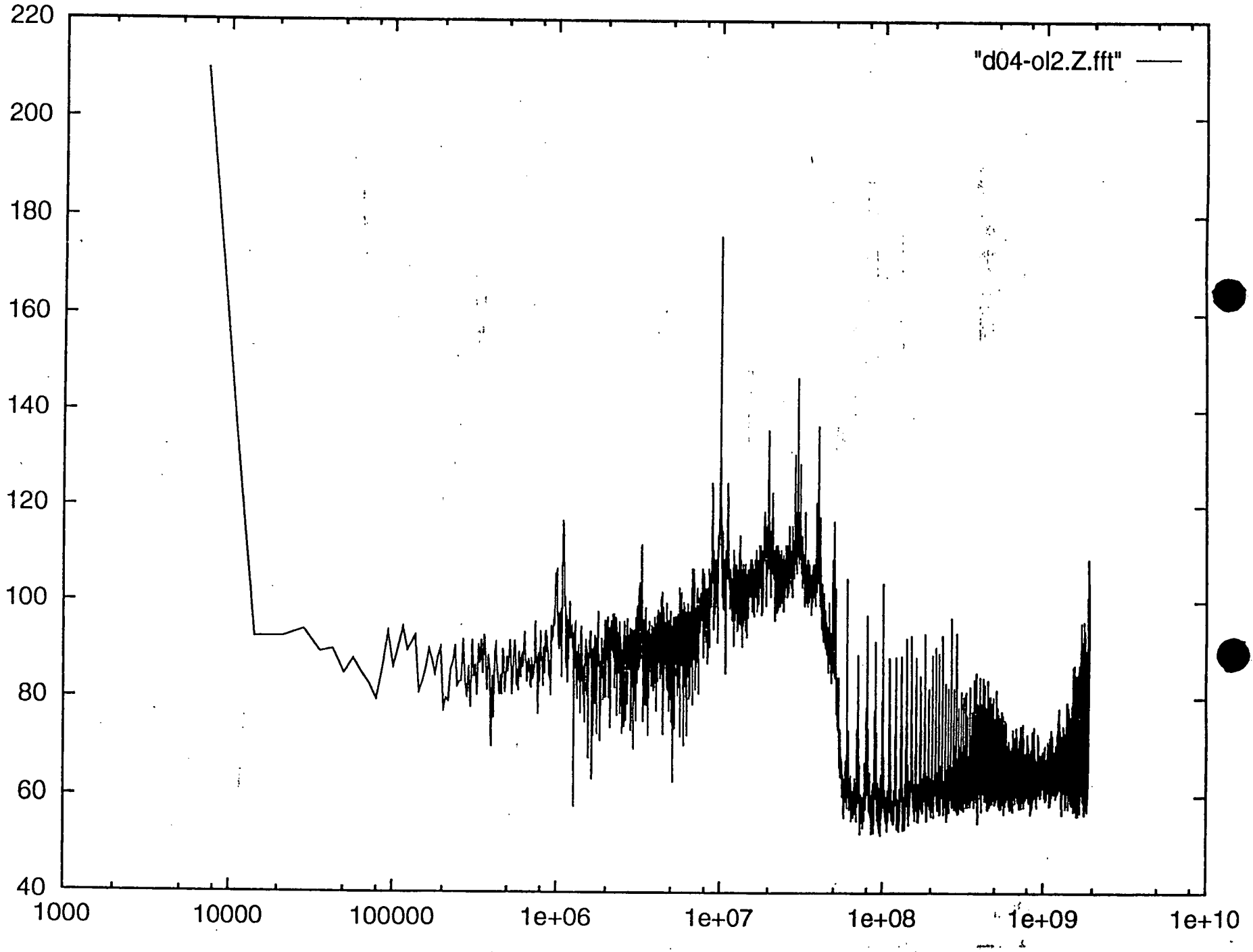
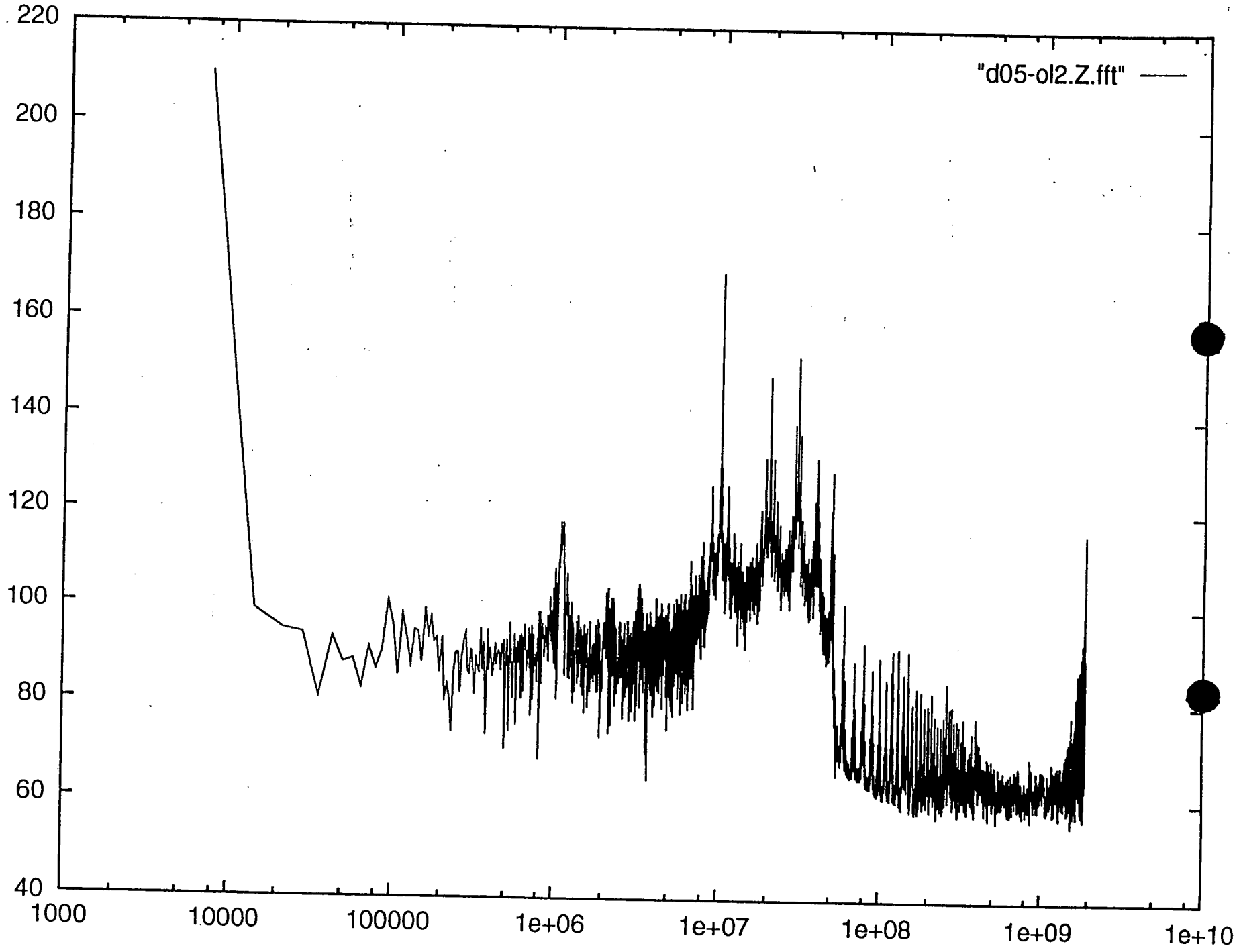
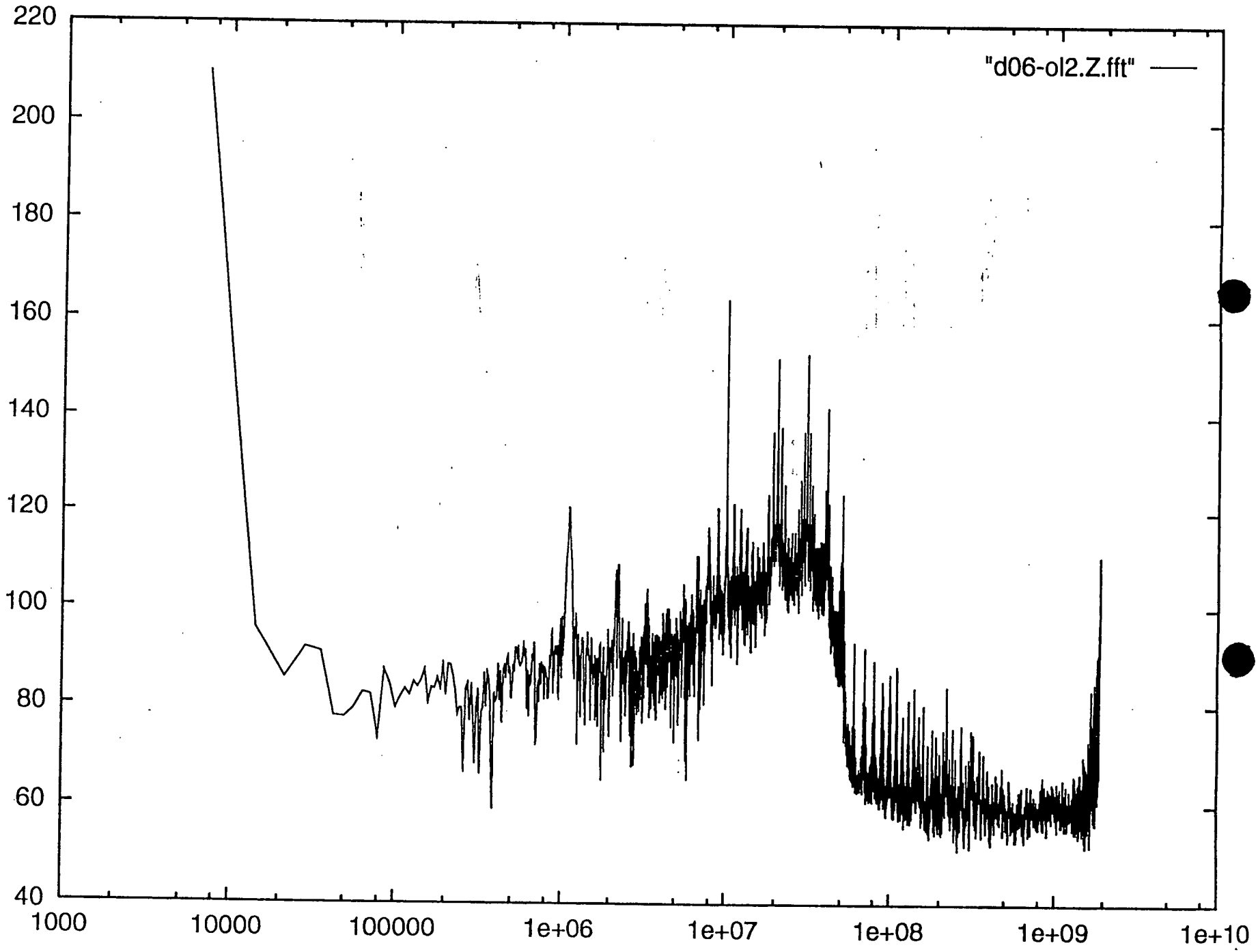
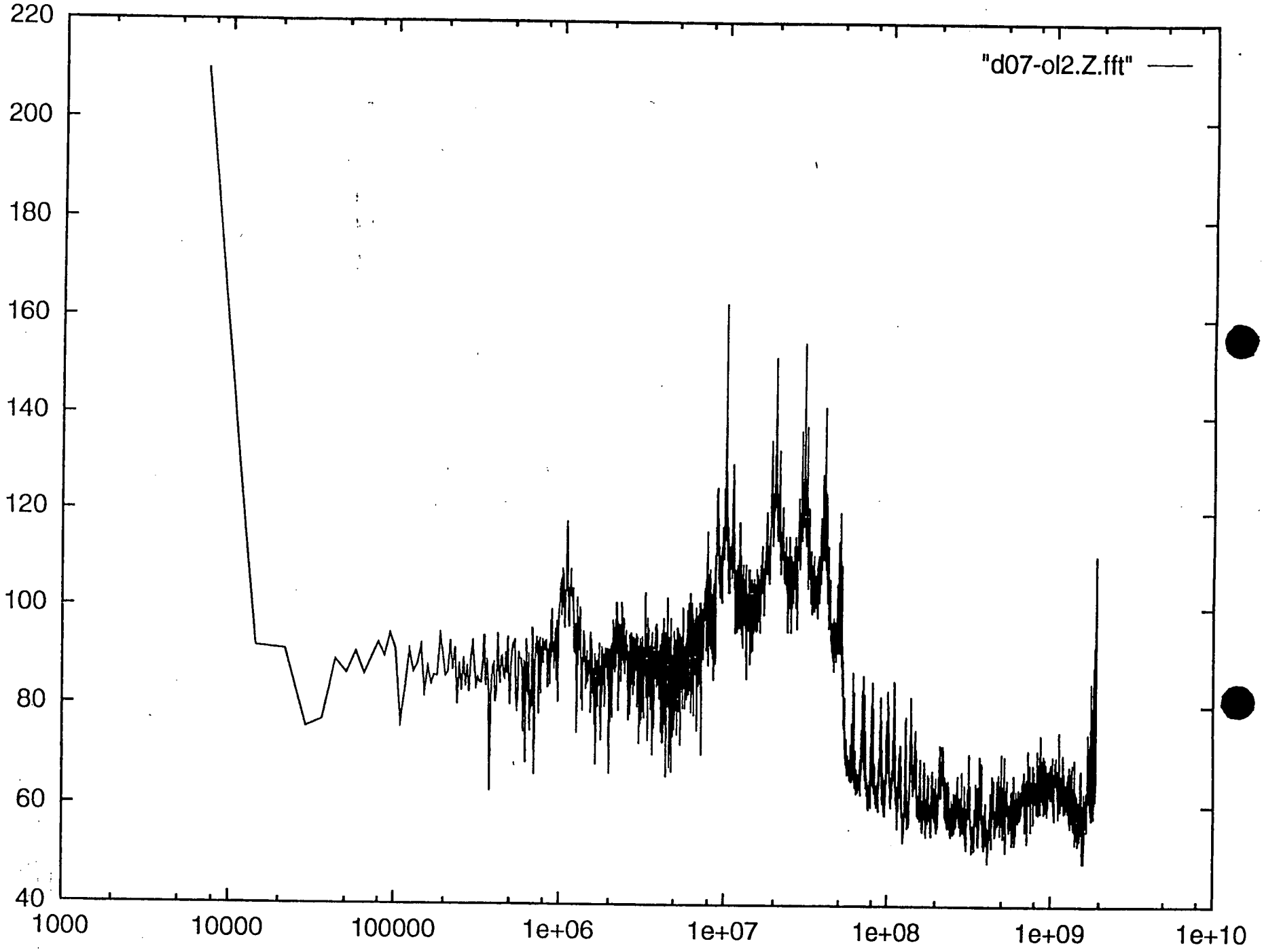
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10


"d03-ol2.Z.fft"
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10


"d04-ol2.Z.fft"
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10


"d05-ol2.Z.fft"
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10


"d06-ol2.Z.fft"
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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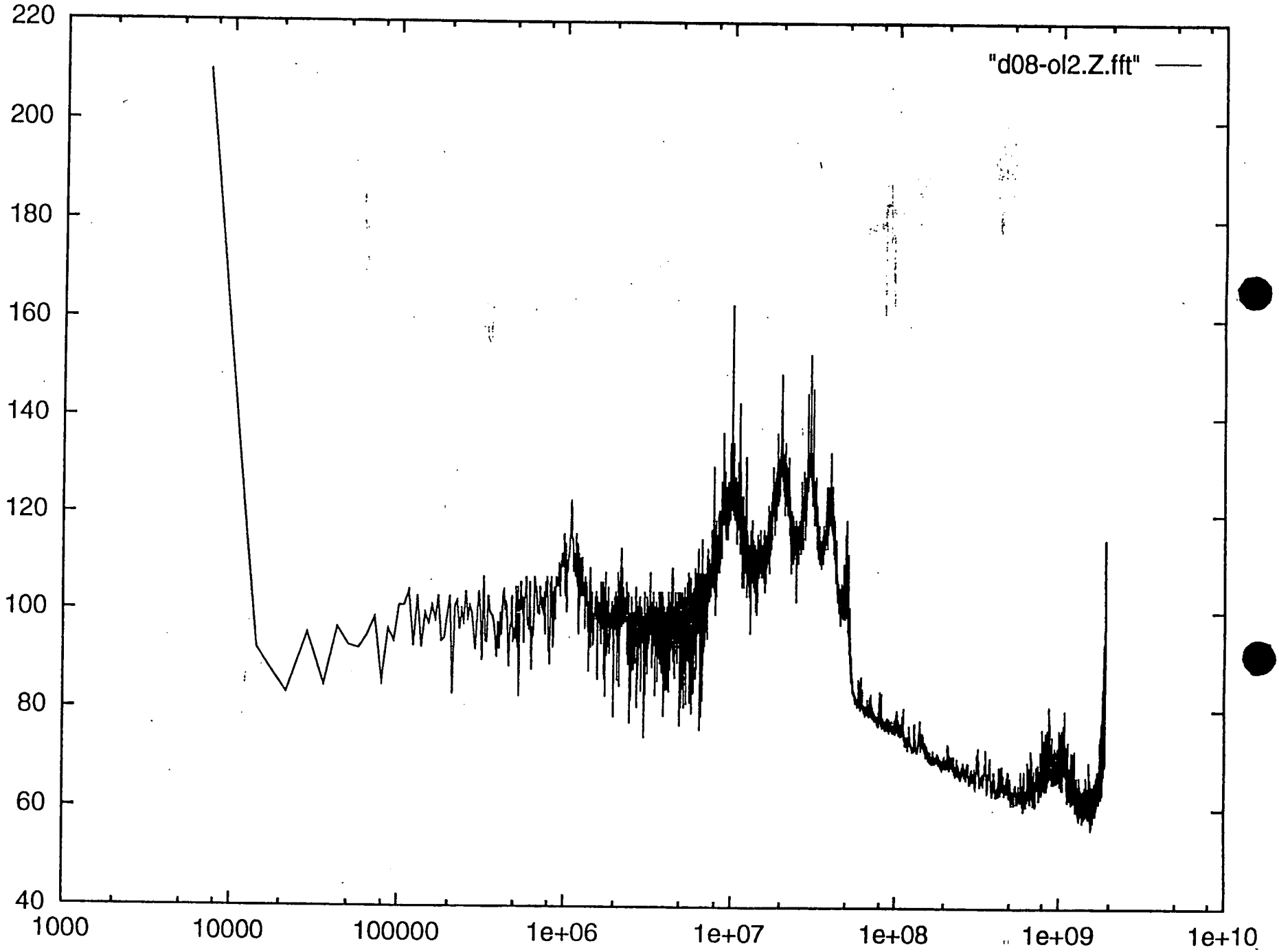
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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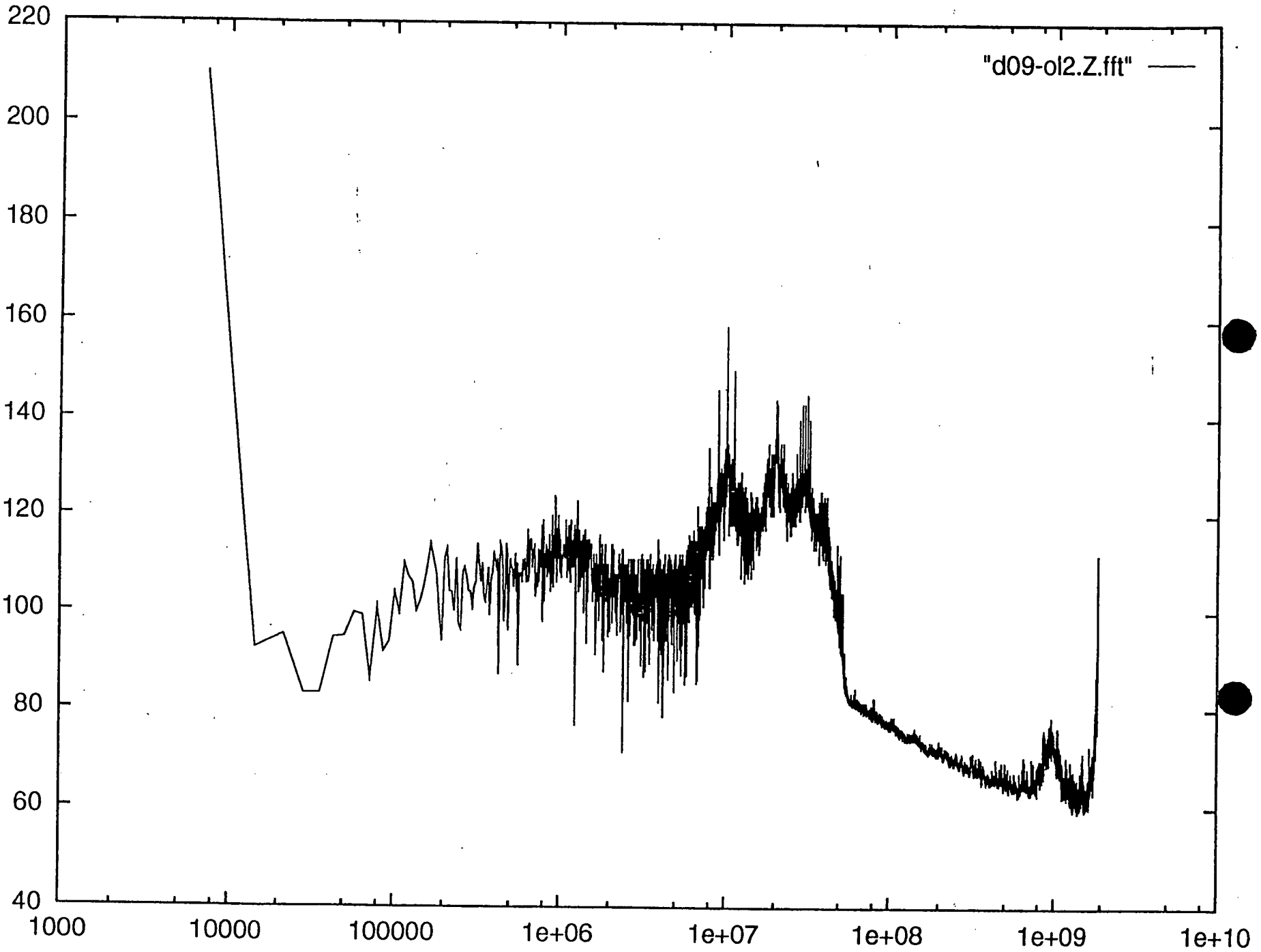
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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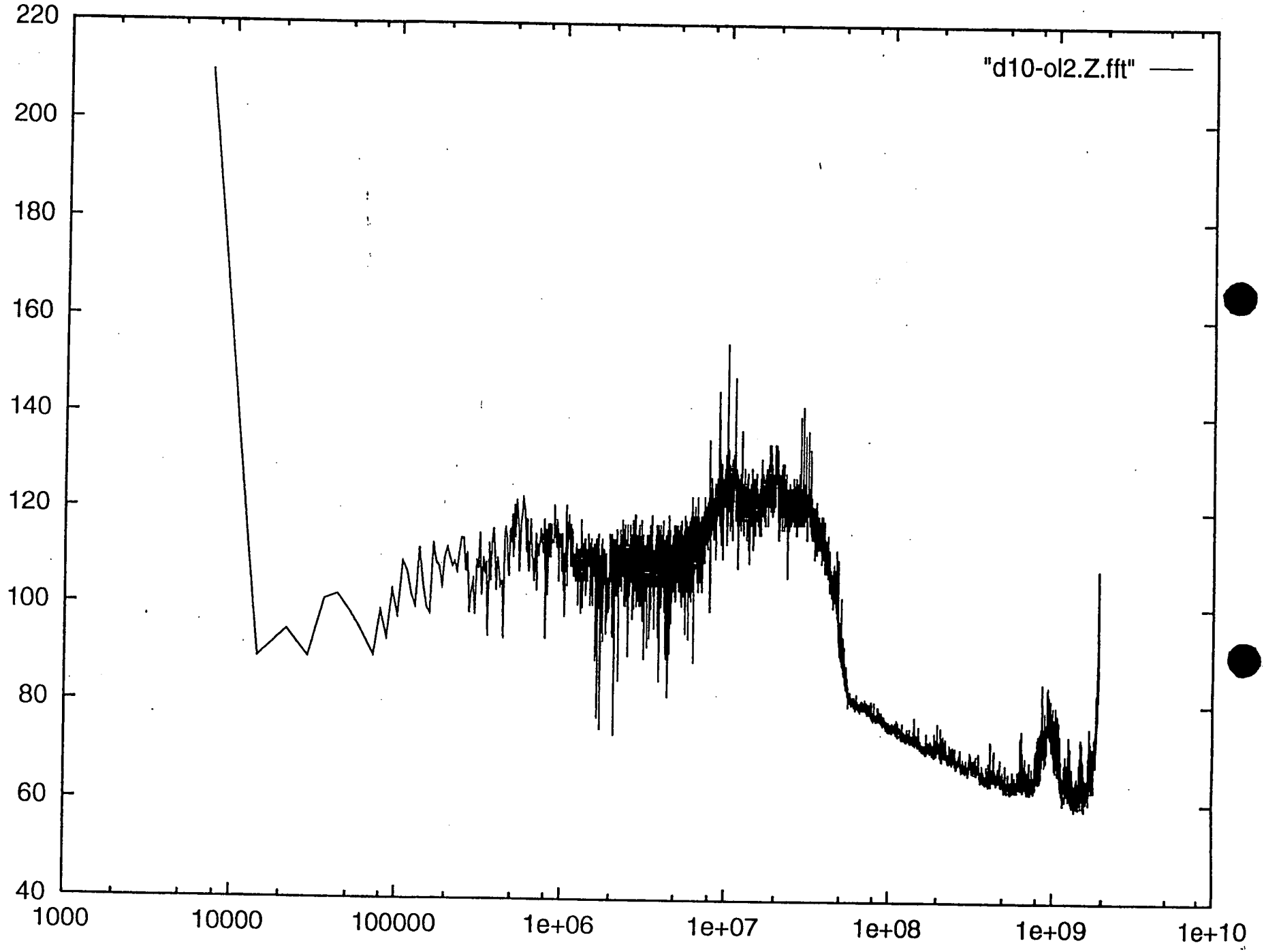
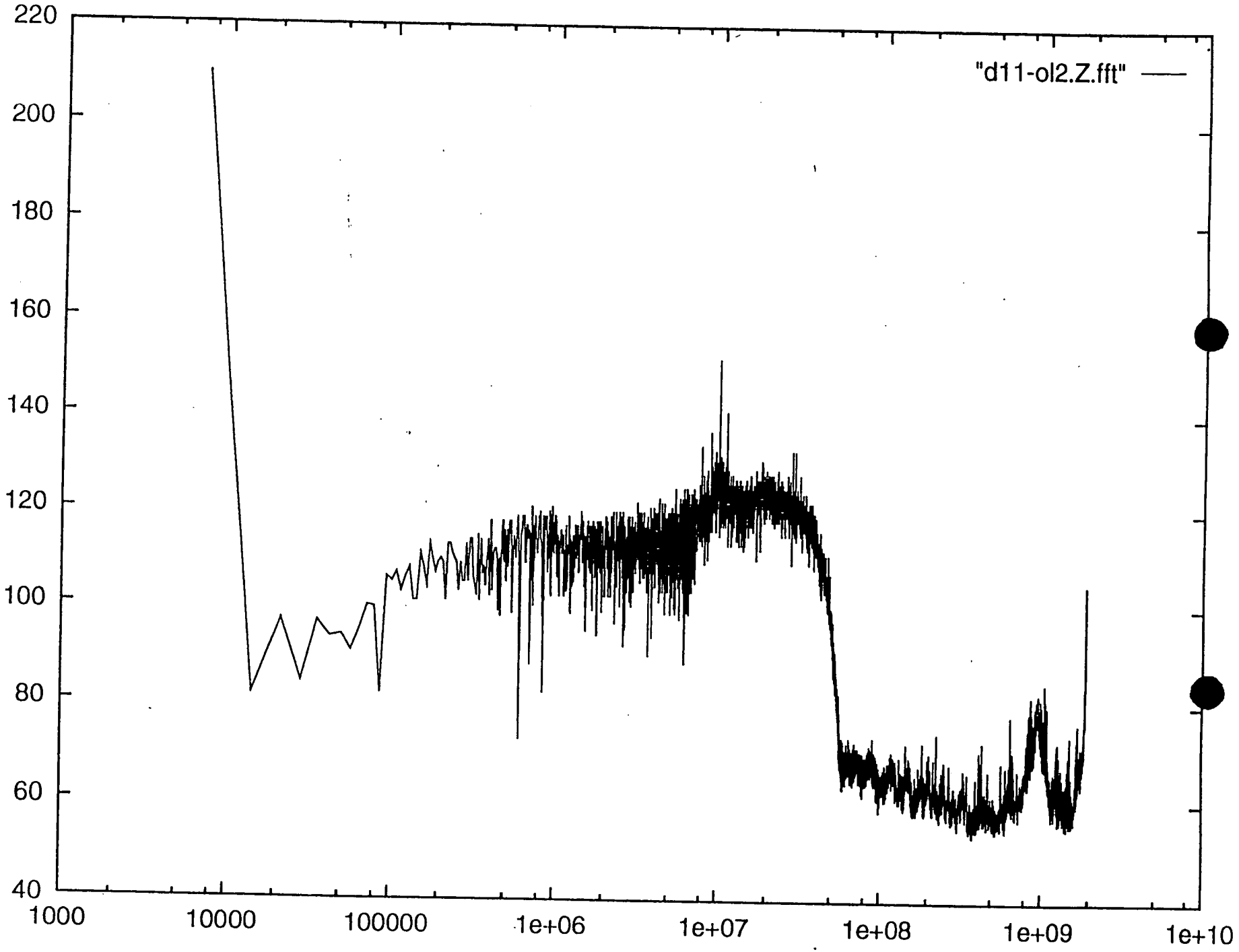
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10


"d10-ol2.Z.fft"
220
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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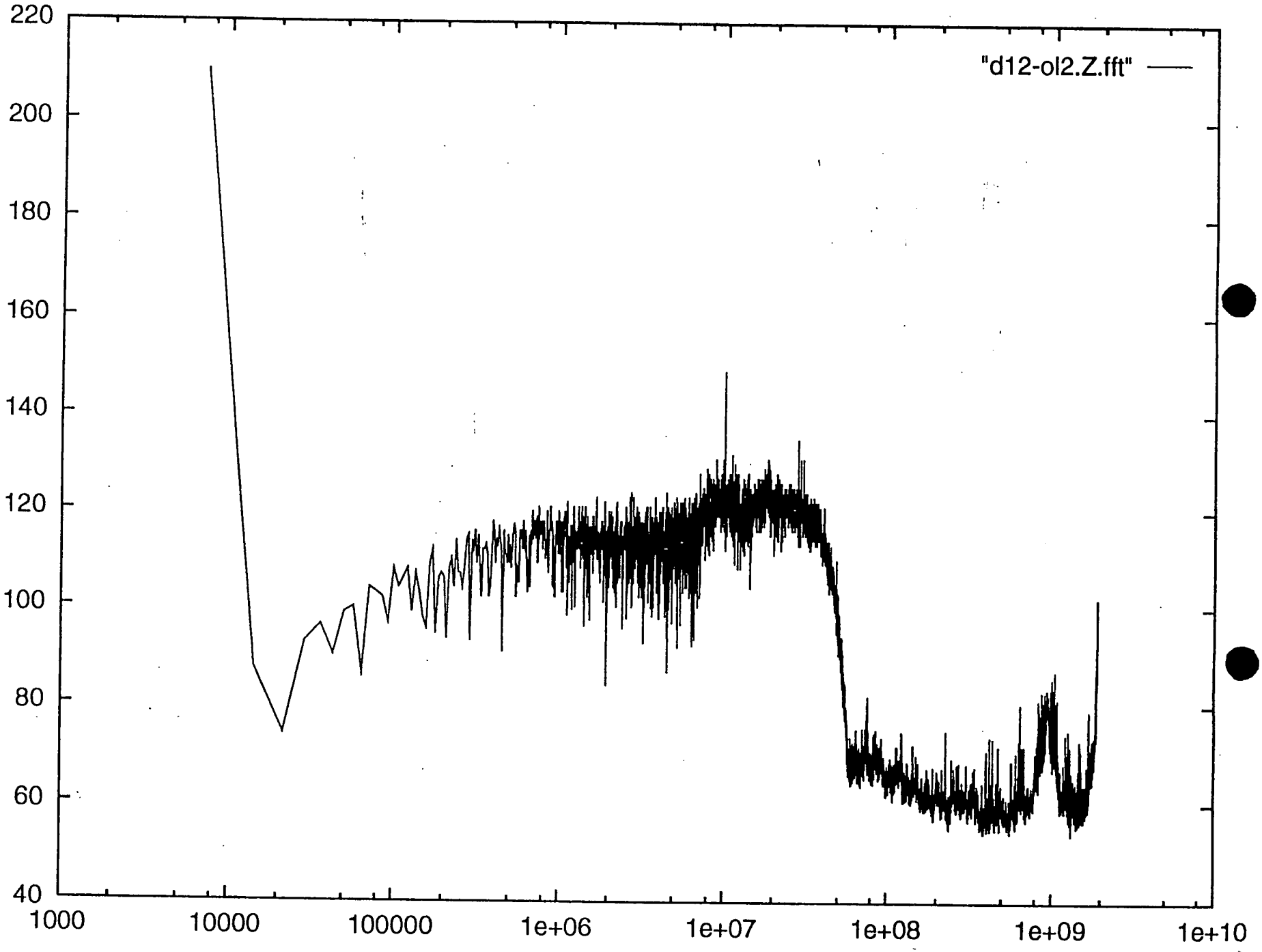
200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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160
140
120
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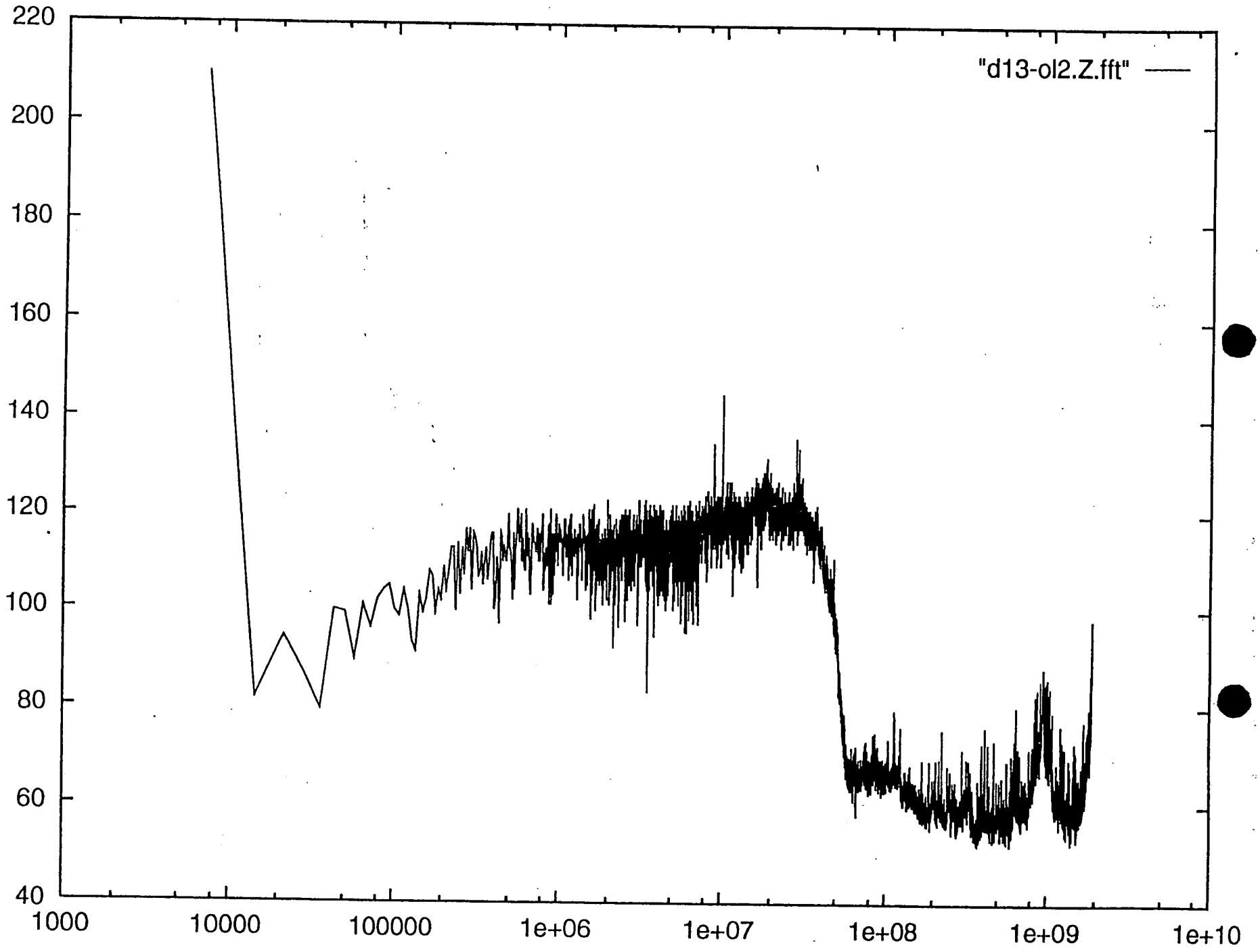
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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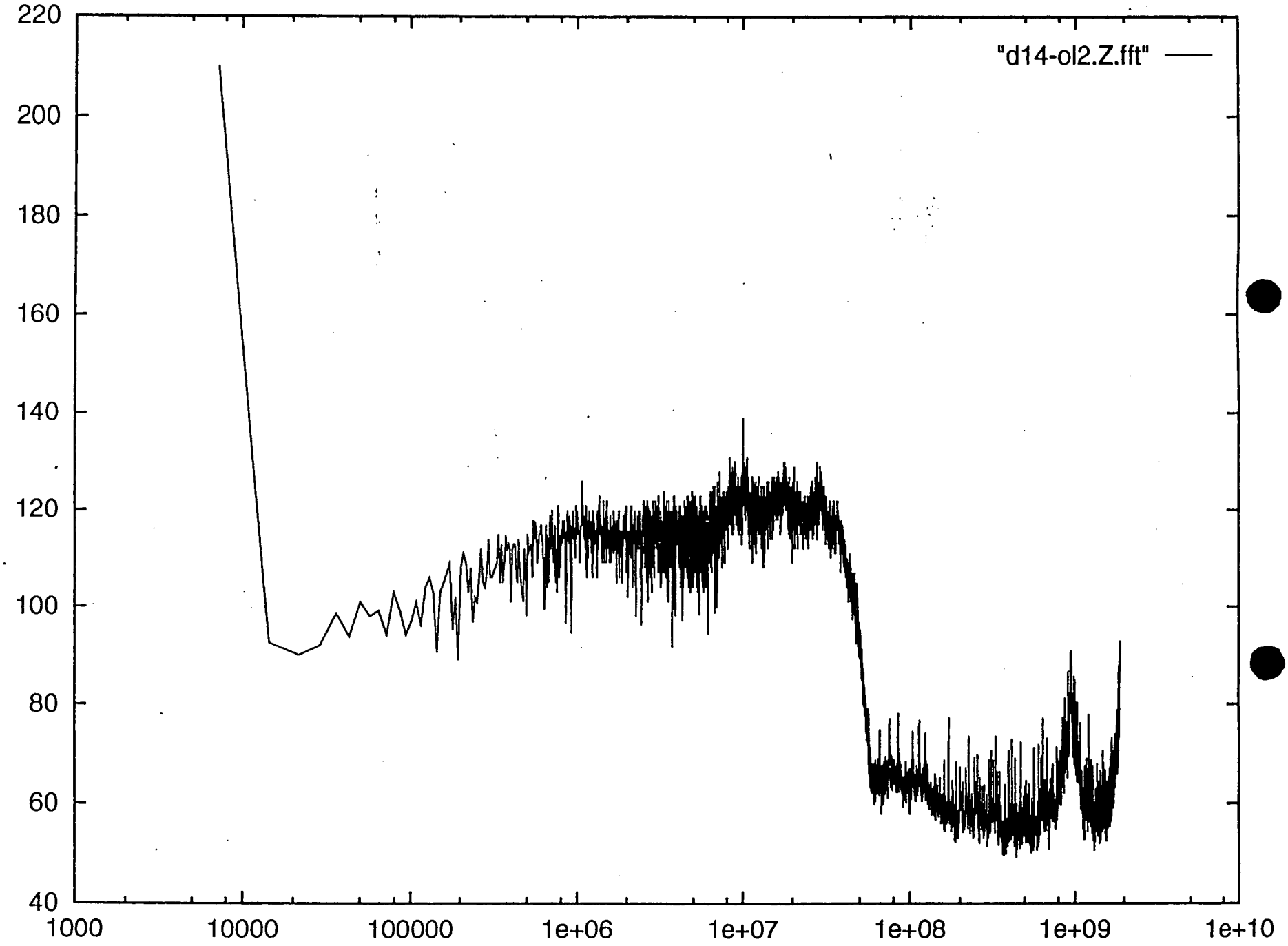
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10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200
180
160
140
120
100
80
60
40
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
1e+10

Plot of output signal to input signal for downconverting sigma-delta modulator

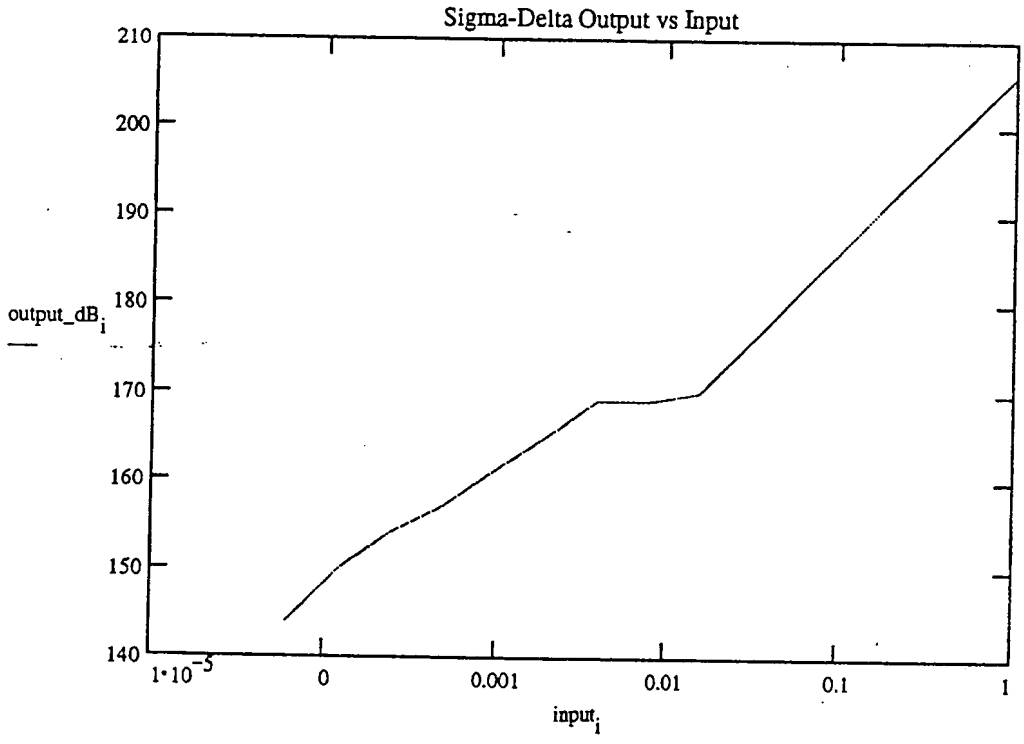
$i := 0..14$

$input_i :=$

1
.5
.25
.125
.0625
.03125
.015625
.0078125
.00390625
.001953125
.0009765625
.000488281
.000244141
.00012207
.000061035

$output\_dB_i :=$

206
200
194
188
182
176
170
169
169
165
161
157
154
150
144



8. Appendix D

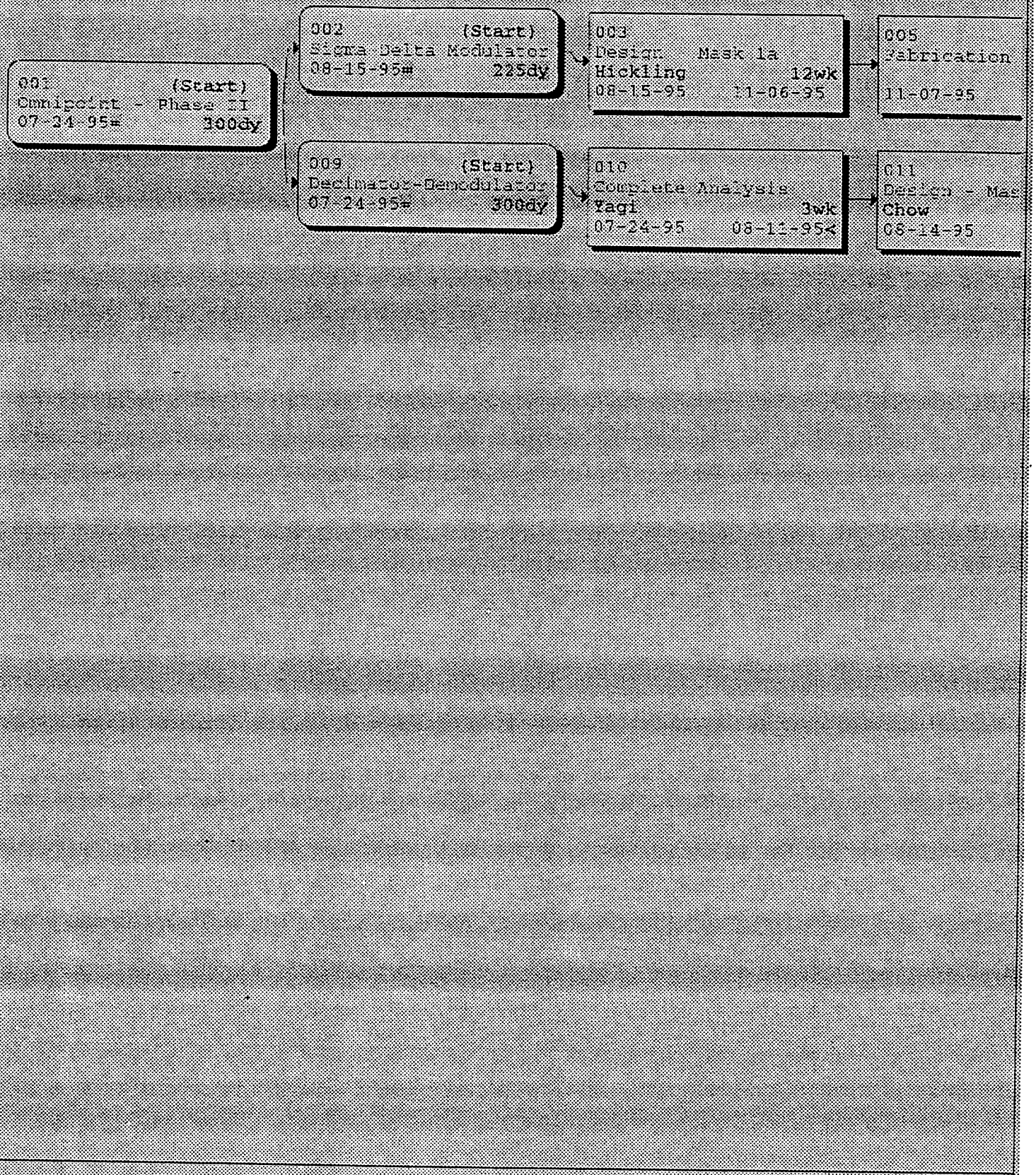
A PERT chart of the proposed two chip development effort.

Exhibit 2

PERT Chart
07-25-95

Omnipoint Project

Project: TECHNOC.PJ
Revision: 10



	Crit	NonCr		
Task box	:	:	Crit link	:
Heading box	:	:	Noncrit link	:
Milestone box	:	:	Select color	:
Subproject box	:	:	Nonselect color	:

PERT Chart
07-25-95

Omnipoint Project

Project: TECHNOC.PJ
Revision: 10